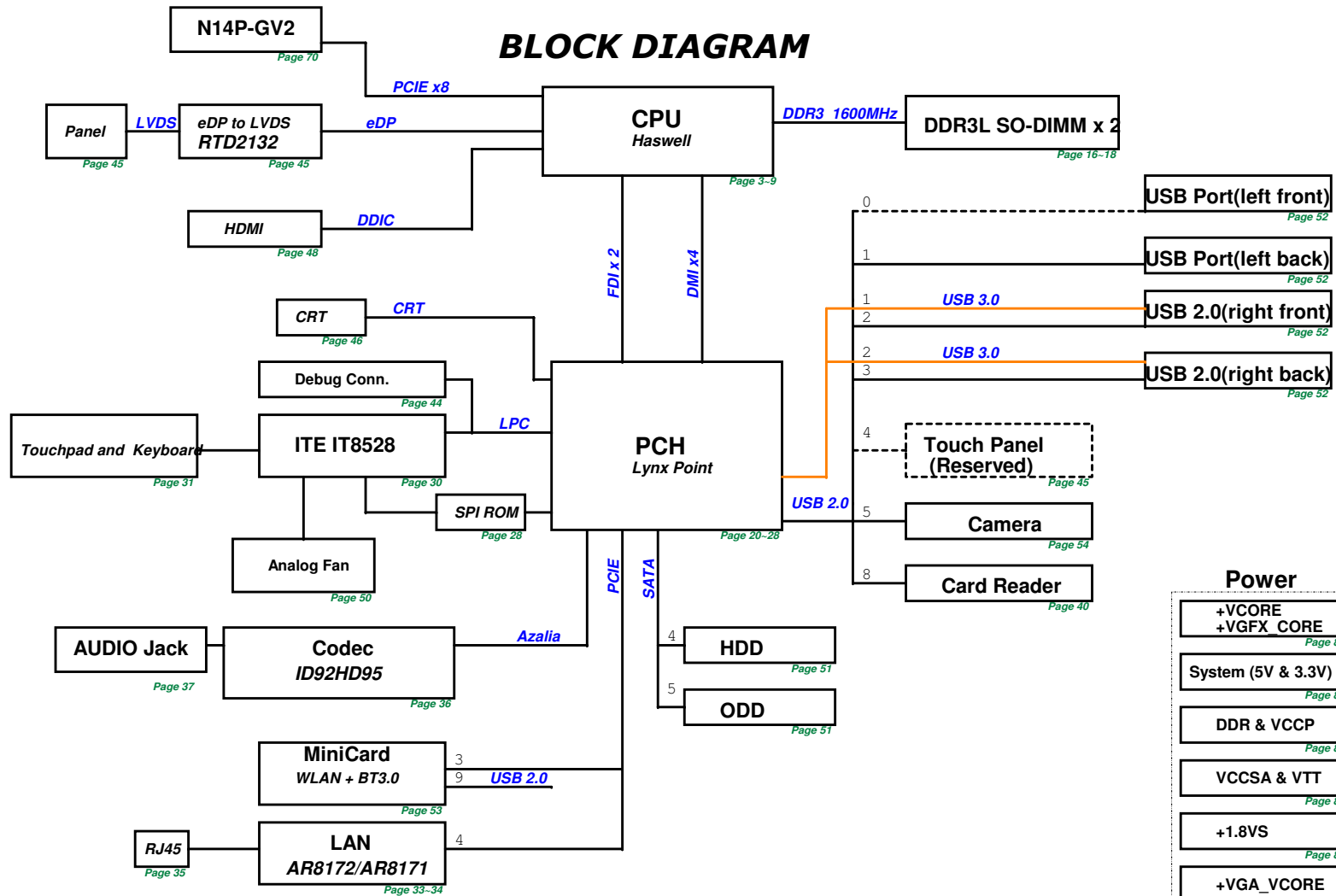


BLOCK DIAGRAM



```

graph TD
    A["+VCORE  
+VGFX_CORE"] --> B[System (5V & 3.3V)]
    B --> C[DDR & VCCP]
    C --> D[VCCSA & VTT]
    D --> E["+1.8VS"]
    E --> F["+VGA_VCORE"]
    F --> G[BATTERY CHARGER]
    G --> H[DETECT]
    H --> I[LOAD SWITCH]
    I --> J[Power Protect]
  
```

+VCORE
+VGFX_CORE *Page 80*

System (5V & 3.3V) *Page 81*

DDR & VCCP *Page 82*

VCCSA & VTT *Page 83*

+1.8VS *Page 84*

+VGA_VCORE *Page 87*

BATTERY CHARGER *Page 88*

DETECT *Page 90*

LOAD SWITCH *Page 91*

Power Protect *Page 92*

Skew Holes

PCH_CPT
GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00		PCB_ID2	EXT PD REV PU	+3VS
GPIO 01		PCB_ID3	EXT PD REV PU	+3VS
GPIO 02		PCB_ID10	REV PU REV PD	+3VS
GPIO 03		SATA_ODD_DA#	EXT PU	+3VS
GPIO 04		PCB_ID11	REV PU REV PD	+3VS
GPIO 05		PCB_ID8	EXT PU REV PD	+3VS
GPIO 06		PCB_ID4	EXT PU REV PD	+3VS
GPIO 07		PCB_ID5	REV PU REV PD	+3VS
GPIO 08		GPIO8	REV PU REV PD	+3VSUS_ORG
GPIO 09		OC5#/GPIO9	EXT PU	+3VSUS_ORG
GPIO 10		OC1#/GPIO10	EXT PU	+3VSUS_ORG
GPIO 11		SMLA_ALERT#	EXT PU	+3VSUS_ORG
GPIO 12		PM_LANPHY_EN	EXT PU	+3VSUS_ORG
GPIO 13		EXT_SCI#	EXT PU	+3VSUS_ORG
GPIO 14		OC7#/GPIO14	EXT PU	+3VSUS_ORG
GPIO 15		EXT_SMI#	EXT PU	+3VSUS+ORG
GPIO 16		GPIO16	EXT PU	+3VS
GPIO 17		DGPU_PWROK	EXT PU	+3VS
GPIO 18		CLK_REQ1#	EXT PU	+3VS
GPIO 19		BBS_RIT0_B	REV PU REV PD	+3VS
GPIO 20		CLK_REQ_WLAN#	EXT PU REV PD	+3VS
GPIO 21		SATA_DET0_R_N	EXT PU	+3VS
GPIO 22		WLAN_LED	EXT PD	
GPIO 23		SNN_LPC_DRQ#1	T2133	
GPIO 24		BT_ON/OFF#	EXT PU REV PD	+3VSUS+ORG
GPIO 25		CLK_REQ_LAN#	EXT PU REV PD	+3VSUS_ORG
GPIO 26		CLK_REQ#4	EXT PU	+3VSUS_ORG
GPIO 27		GPIO27	REV PU	+VCCDSW
GPIO 28		WLAN_ON	EXT PU	+3VSUS_ORG
GPIO 29		SLP_WLAN#	T2205	
GPIO 30		SUS_PWR_ACK_R	EXT PU	+3VSUS_ORG
GPIO 31		AC_PRESENT_R	EXT PU	+VCCDSW
GPIO 33		HDA_DOCK_EN#	T2001	
GPIO 34		+15_TV_PWRGD	EXT PU	+3VS
GPIO 35		CR2_IN#	EXT PU	+3VS
GPIO 36		GPIO36	EXT PD	
GPIO 37		FDI_OVRVLIT	EXT PD REV PU	+3VS
GPIO 38		PCB_ID0	EXT PD REV PU	+3VS
GPIO 39		PCB_ID1	REV PU EXT PD	+3VS
GPIO 40		OC1#/GPIO40	EXT PU	+3VSUS_ORG
GPIO 41		OC2#/GPIO41	EXT PU	+3VSUS_ORG
GPIO 42		OC3#/GPIO42	EXT PU	+3VSUS_ORG
GPIO 43		OC4#/GPIO43	EXT PU	+3VSUS_ORG
GPIO 44		CLK_TV_REQ#	EXT PU	+3VSUS_ORG
GPIO 45		CLK_REQ#6	EXT PU	+3VSUS_ORG
GPIO 46		CLK_REQ#7	EXT PU	+3VSUS_ORG
GPIO 47		CLKREQ_PEG#	EXT PU	+3VSUS_ORG
GPIO 48		PCB_ID6	REV PU REV PD	+3VS
GPIO 49		SATA_ODD_PRSNT#_R	EXT PU	+3VS
GPIO 50		DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 51		BBS_RIT1	REV PU REV PD	+3VS
GPIO 52		PCB_ID9	REV PU REV PD	+3VS
GPIO 53		DGPU_PWM_SELECT#	REV PU	+3VS
GPIO 54		VGA_PWRON	EXT PU	+3VS
GPIO 55		STP_AL6OVR	REV PD	
GPIO 56		CLK_REQ_PEG_B#	EXT PU	+3VSUS_ORG
GPIO 57		GPIO57	REV PU	+3VSUS_ORG
GPIO 58		SML1_CLK	EXT PU	+3VSUS_ORG
GPIO 59		OC0#/GPIO59	EXT PU	+3VSUS_ORG
GPIO 60		DRAMST_CNTRL_PCH	EXT PU	+3VSUS_ORG
GPIO 61		PM_SUS_STAT#	T2203	
GPIO 62		SUSCLK_C	REV PD	
GPIO 63		SLP_S#	T2204	
GPIO 64		KB_LED_ID	T2111	
GPIO 65		CLK_USB4#_CR_K		
GPIO 66		PCB_ID14	EXT PU REV PD	+3VS
GPIO 67		PCB_ID12	REV PU REV PD	+3VS
GPIO 68		SATA_ODD_PWRGT	REV PU	+3VS
GPIO 69		LNb_EN	EXT PU	+3VS
GPIO 70		GPIO70	REV PU REV PD	+3VS
GPIO 71		PCB_ID7	EXT PU REV PD	+3VS
GPIO 72		GPIO72	EXT PU	+VCCDSW
GPIO 73		CLK_REQ0#	EXT PU	+3VSUS_ORG
GPIO 74		SML1_ALERT#	EXT PU	+3VSUS_ORG
GPIO 75		SML1_DAT	EXT PU	+3VSUS_ORG

EC
ITE8528

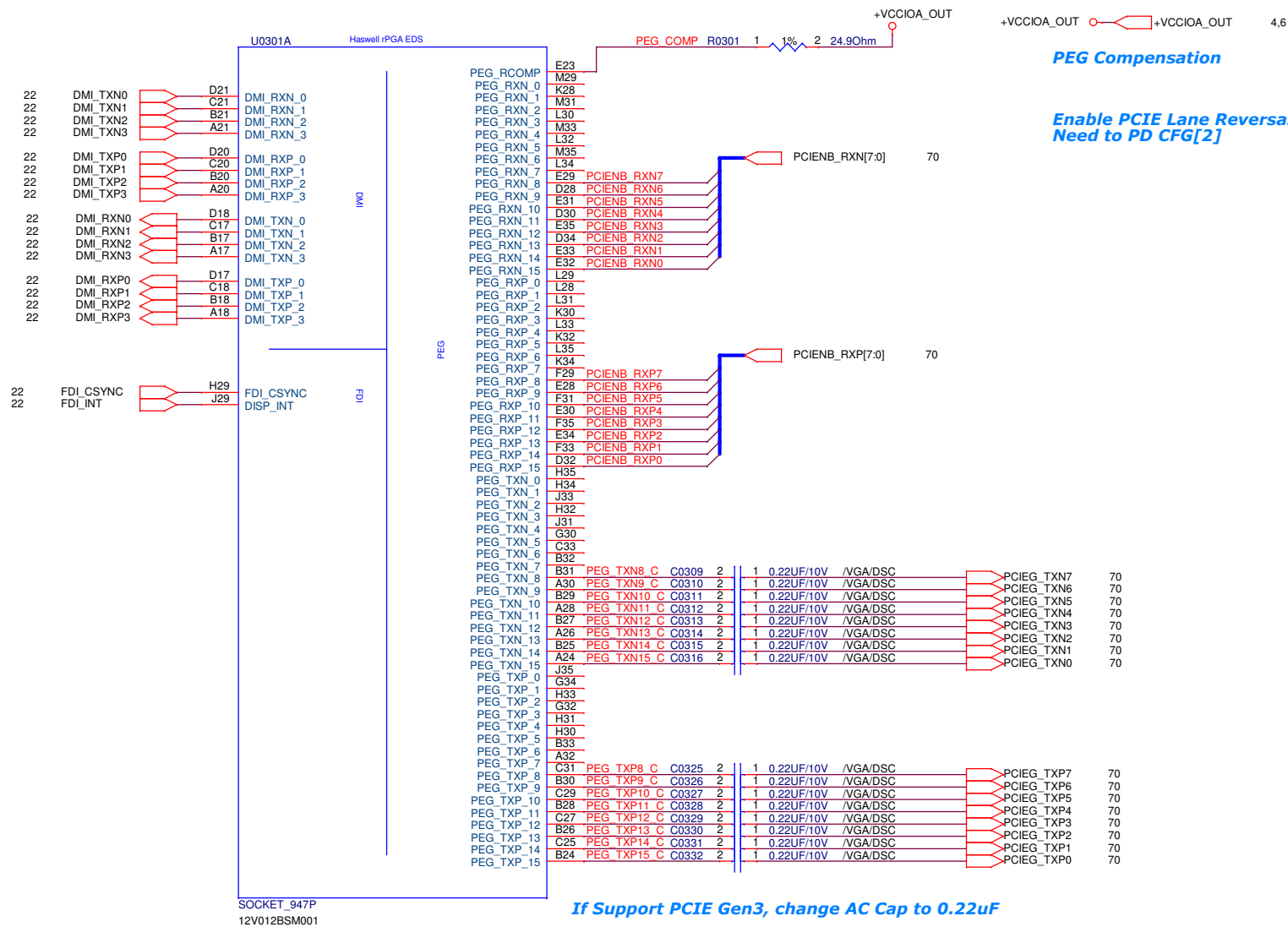
EC GPIO	Use As	Signal Name
GPIO0		PWR_WHITE_LED#
GPIO1		BAT_ORG_LED#
GPIO2		AOAC_RST#(test_point)
GPIO3		AC_IN_LED#
GPIO4		FB_CLAMP_TGL_REQ#
GPIO5		CHGCB2#
GPIO6		THERM_ALERT#_EC
GPIO7		PCH_FLASH_DESCRIPTOR
GPIO8		NUM_LED#
GPIO1		CAP_LED#
GPIO2		THRO_CPU
GPIO3		SMB1_CLK
GPIO4		SMB0_DAT
GPIO5		A20GATE
GPIO6		RCIN#
GPIO7		PM_RSMRST#
GPIO0		RF_ON(Test_point)
GPIO1		SMB1_CLK
GPIO2		SMB1_DAT
GPIO3		KS016
GPIO4		AC_IN_OC
GPIO5		KS017
GPIO6		BAT1_IN_OC#
GPIO7		ME_AC_PRESENT
GPIO0		PM_SUSB#
GPIO1		PM_SUSB#
GPIO2		BUF_PLT_RST#
GPIO3		EXT_SCI#
GPIO4		EXT_SMI#
GPIO5		PM_PWRK
GPIO6		FAN0_TACH
GPIO7		USBP01_EN
GPIO0		V5SUS_ON
GPIO1		SUSC_EC#
GPIO2		SUSC_ECP
GPIO3		CPU_VRON
GPIO4		PWR_SW#_M
GPIO5		USB_OC01#_EC
GPIO6		LID_SW#
GPIO7		USB_OC2#_EC
GPIO0		BAT_LEARN
GPIO1		ME_SUSPWRDNACK
GPIO2		PM_PWRBTN#
GPIO3		SUSACK#(test_point)
GPIO4		TP_CLK
GPIO5		TP_DAT
GPIO6		H_PECI_EC
GPIO7		LCD_BACKOFF#
GPIO0		HDMI_RPD_M
GPIO1		FDIO2(Test_point)
GPIO2		AOAC_PWRON(Test_point)
GPIO6		FDIO3(Test_point)
GPIO0		PM_CLKRUN#
GPIO1		CHGCB0#
GPIO2		CHGCB1#
GPIO3		SPI_CS#1
GPIO4		SPI_CLK
GPIO5		SPI_SO
GPIO6		SPI_SI
GPIO0		AD_T1NP
GPIO1		SUS_PWRGD
GPIO2		ALL_SYSTEM_PWRGD
GPIO3		VRM_PWRGD
GPIO4		ADAPT_AD
GPIO5		EC_SLP_SUS#(Test_point)
GPIO6		WLAN_WAK#(Test_point)
GPIO7		INON(Test_point)
GPIO0		HDIO2(Test_point)
GPIO1		HDIO3(Test_point)
GPIO2		OP_SD#
GPIO3		USBSLP_EN
GPIO4		FB_CLAMP
GPIO5		CTL_FAN
GPIO6		SW_RTCRST
GPIO7		BACK_EN

EC Name	Use As	Signal Name
LAD0		LPC_A00
LAD1		LPC_AD1
LAD2		LPC_AD2
LAD3		LPC_AD3
LCLK		CLK_KBCPC1_PCH
LFRAME#		LPC_FRAME#
LRESET#		BUF_PLT_RST#
SERIRQ		INT_SERIRQ
WRST#		EC_RST#
PECI		H_PECI_EC
F5CK		SCK
FMIO0		IO
FMOSI		SI
FSCE#		SCE#
KSIO		KSIO
KS11		KS11
KS12		KS12
KS13		KS13
KS14		KS14
KS15		KS15
KS16		KS16
KS17		KS17
KS00		KS00
KS01		KS01
KS02		KS02
KS03		KS03
KS04		KS04
KS05		KS05
KS06		KS06
KS07		KS07
KS08		KS08
KS09		KS09
KS010		KS010
KS011		KS011
KS012		KS012
KS013		KS013
KS014		KS014
KS015		KS015

SM_BUS ADDRESS :

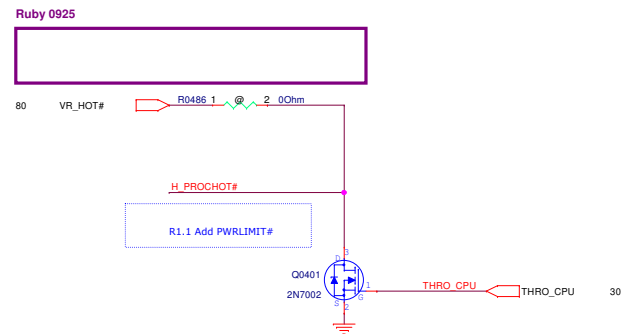
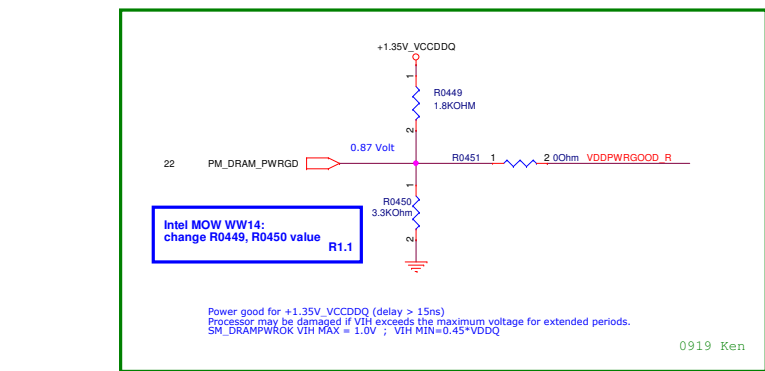
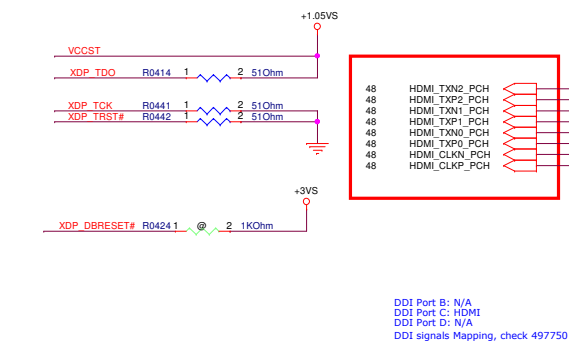
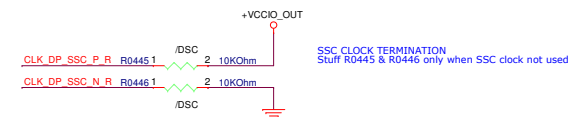
SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	NC	USB 0	USB2.0 Port(Reserve)
PCIE 2	NC	USB 1	USB2.0 Port(debug)
PCIE 3	MiniCard WLAN	USB 2	USB3.0 Port (1)
PCIE 4	LAN	USB 3	USB3.0 Port (2)
PCIE 5	NC	USB 4	Touch Panel (reserve)
PCIE 6	NC	USB 5	Camera
PCIE 7	NC	USB 6	NC
PCIE 8	NC	USB 7	NC
SATA0	NC	USB 8	Card Reader
SATA1	NC	USB 9	WiFi/Max
SATA2	NC	USB 10	NC
SATA3	NC	USB 12	NC
SATA4	SATA HDD	USB 11	NC
SATA5	SATA ODD	USB 13	NC
USB3 1	USB3.0 Port (1)		
USB3 2	USB3.0 Port (2)		
USB3 3	NC		
USB3 4	NC		
USB3 5	NC		
USB3 6	NC		

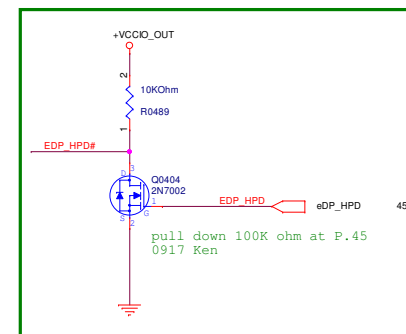


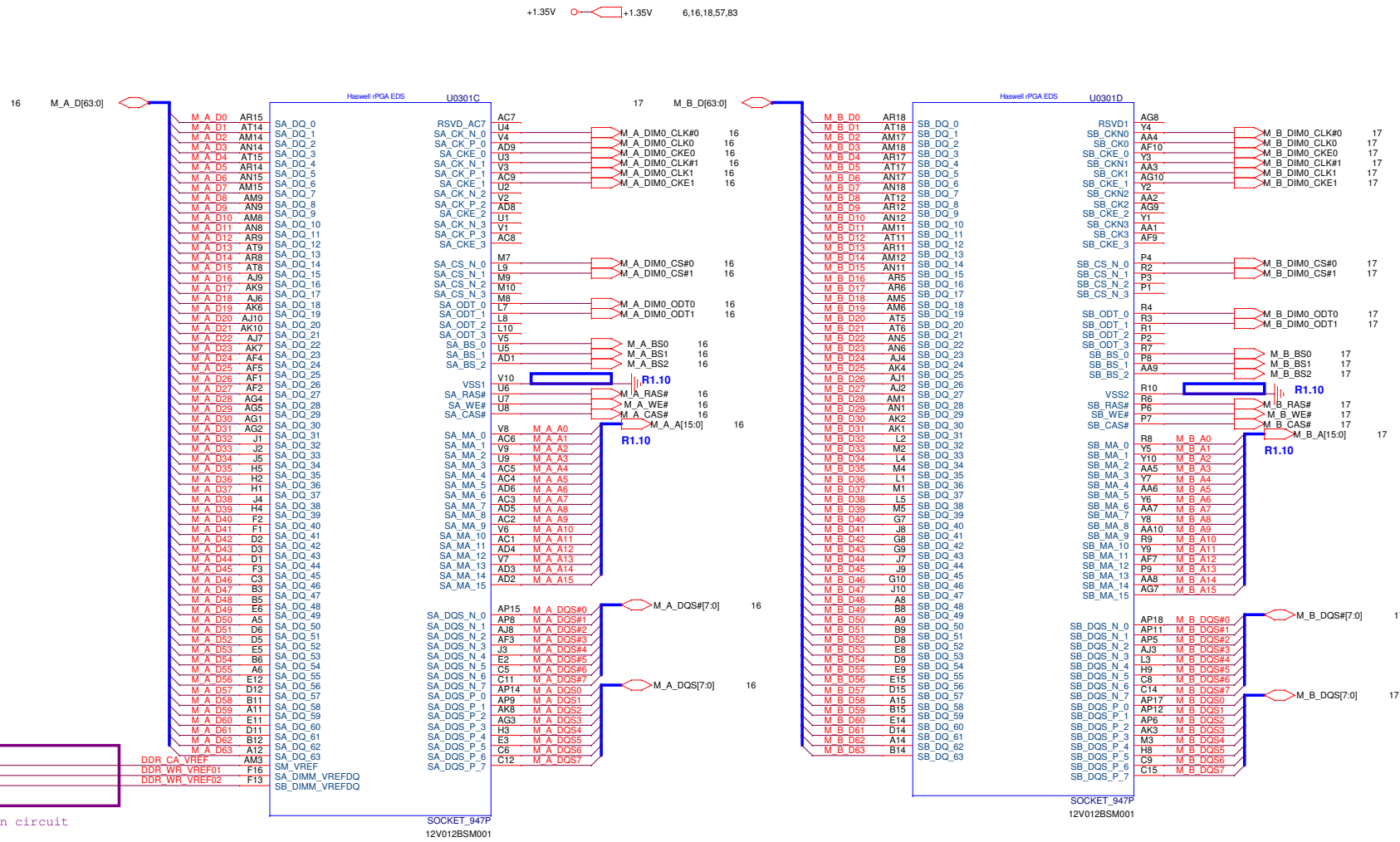
PEGATRON		Title : CPU(1)_DMI,PEG,FDI	
BG1CORE		Engineer: Ruby Tsai	
Size B	Project Name PT10SG		Rev 1.1
Date: Tuesday, February 26, 2013		Sheet 3 of 104	

Stuff R0408
Intel MOW WW14: stuff
H_CUPWRGD PD 10Kohm R1.1



+VCCIO_OUT	6,32,57
+1.35V_VCCDDQ	6
+3VSUS	22,23,27,28,30,33,37,53,81,92
+3V	23,44,45,57,91
+1.05VS	26,27,32,57,80,82
+VCCIOA_OUT	3,6

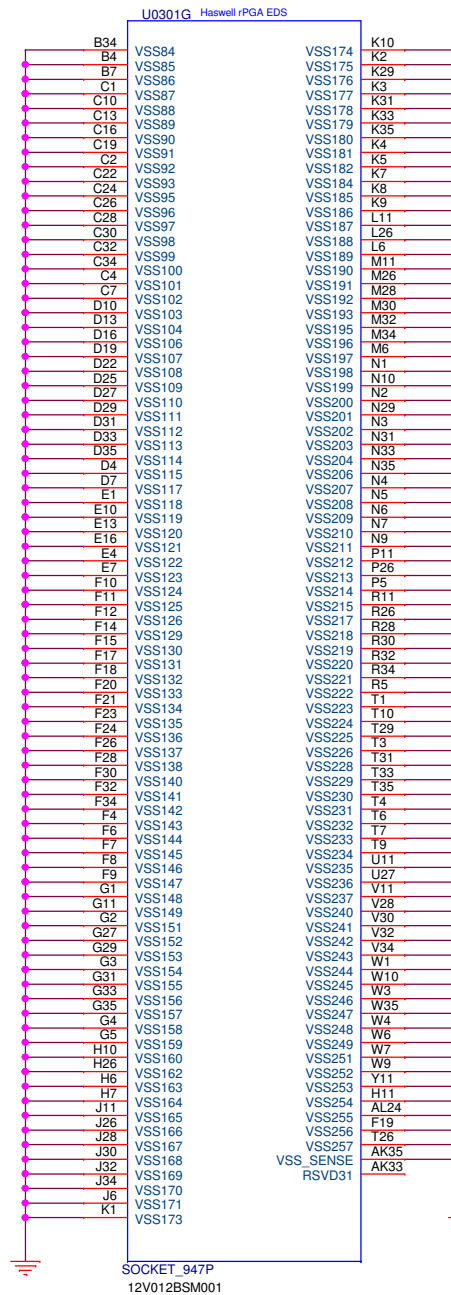
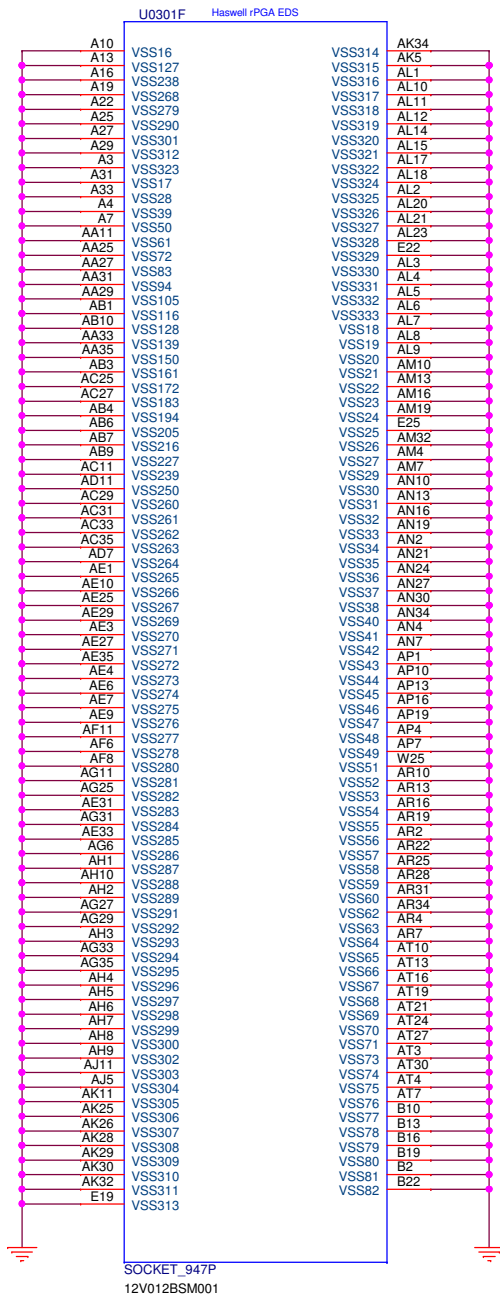




<http://forum.hocvienit.vn>



PEGATRON		Title : CPU(4)_PWR	
BG1CORE		Engineer: Ruby Tsal	
Size Custom	Project Name PT10SG		Rev 1.1
Date: Tuesday, February 26, 2013		Sheet	7 of 104



Placement note:
1. R0801 close to CPU

VSS SENSE R2 R0801 1 00hm VSSSENSE 80

100 ohm in power circuit
0921 Ken

PEGATRON Title : CPU(6)_GND		
BG1/CORE		Engineer: Ruby Tsai
Size B	Project Name PT10SG	Rev 1.1
Date: Tuesday, February 26, 2013	Sheet 8	of 104

CFG strapping information: The CFG signals have a default value of '1'

CFG[1:0]: Reserved configuration lane.

CFG[2]: PCIe Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches socket pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

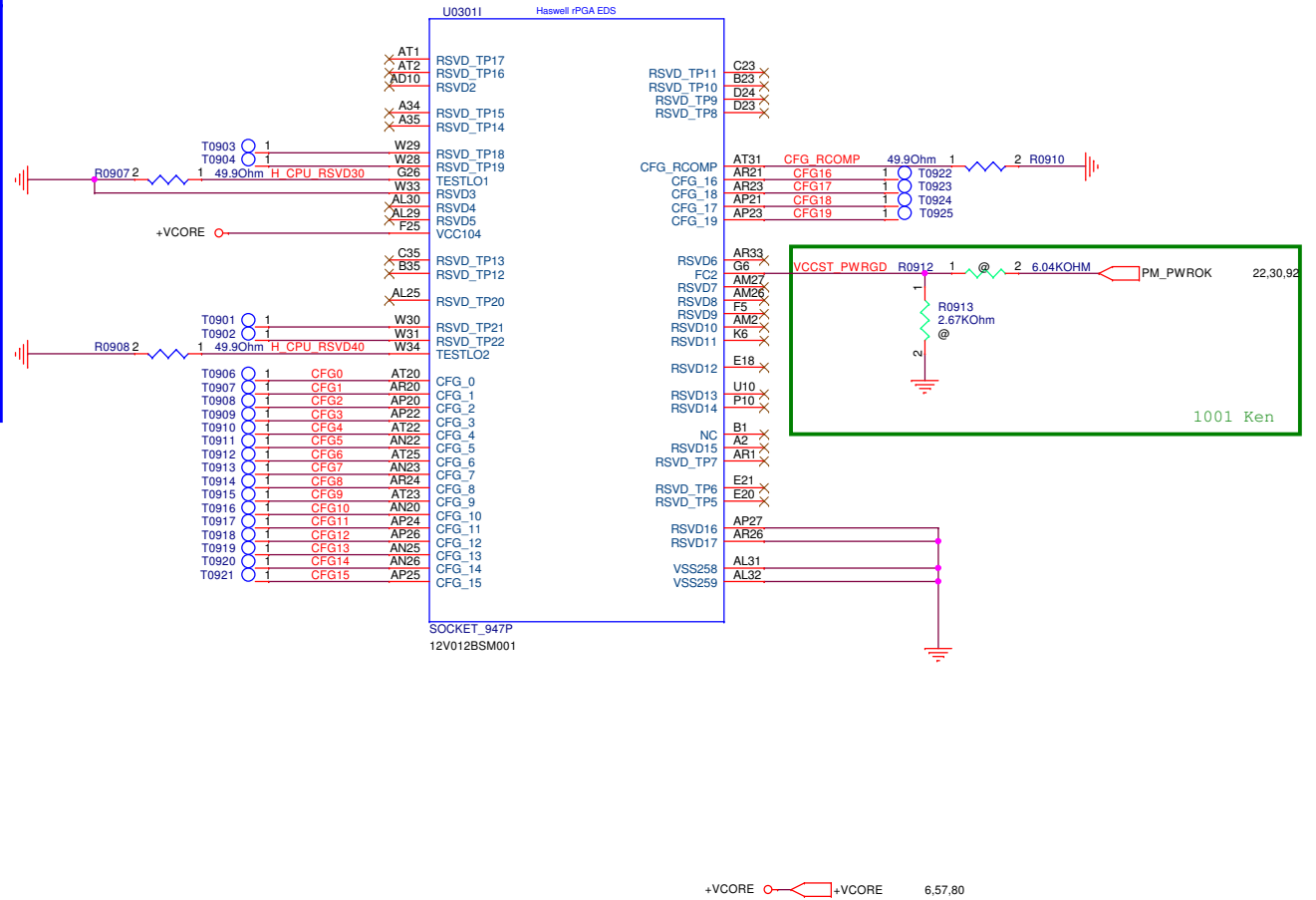
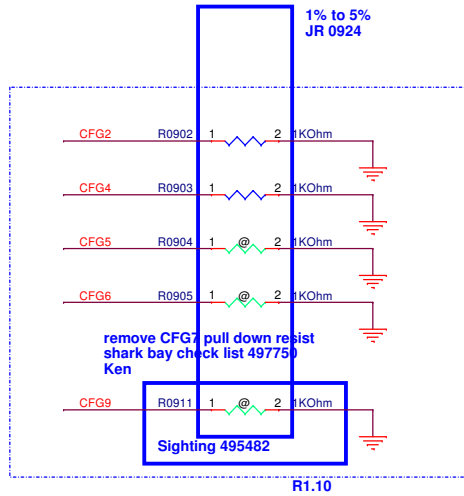
CFG[4]: eDP enable

-1 = Disabled
-0 = Enabled

CFG[6:5]: PCI Express Port Bifurcation Straps

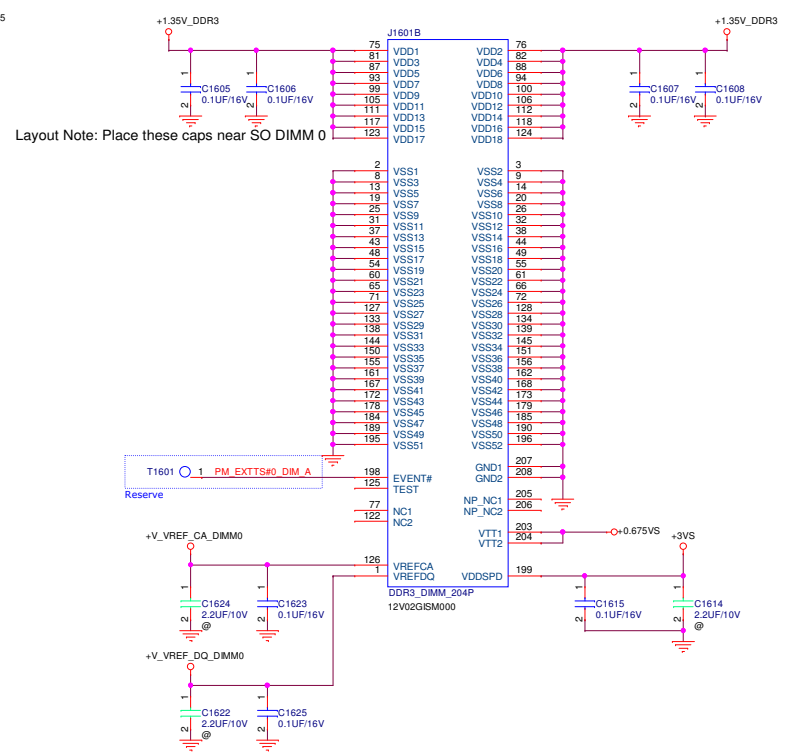
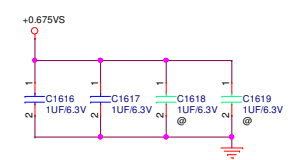
-00 = 1 x8, 2 x4 PCI Express*
-01 = reserved
-10 = 2 x8 PCI Express*
-11 = 1 x16 PCI Express*

CFG[19:7]: Reserved configuration lane.

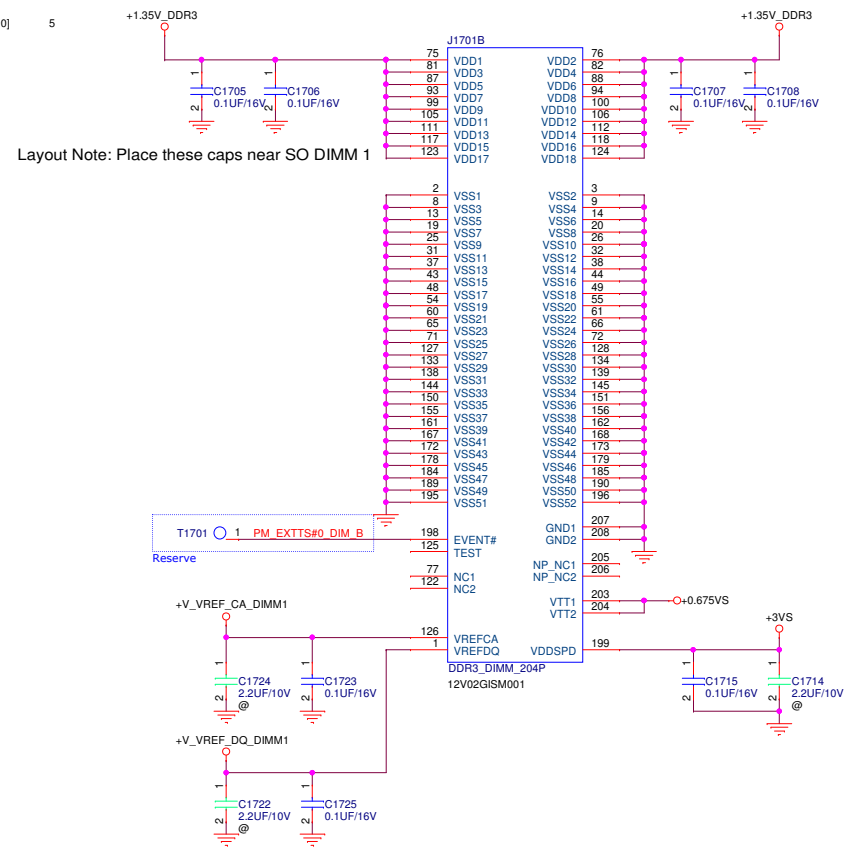
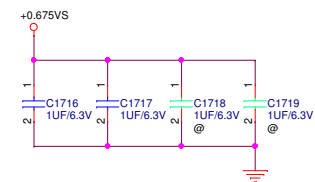


<http://forum.hocvienit.vn>

PEGATRON		Title : CPU_PCH_XDP	
BGHICORE		Engineer: Ruby Tsal	
Size	Project Name		Rev
C	PT10SG		1.1
Date: Tuesday, February 26, 2013		Sheet	10 of 104



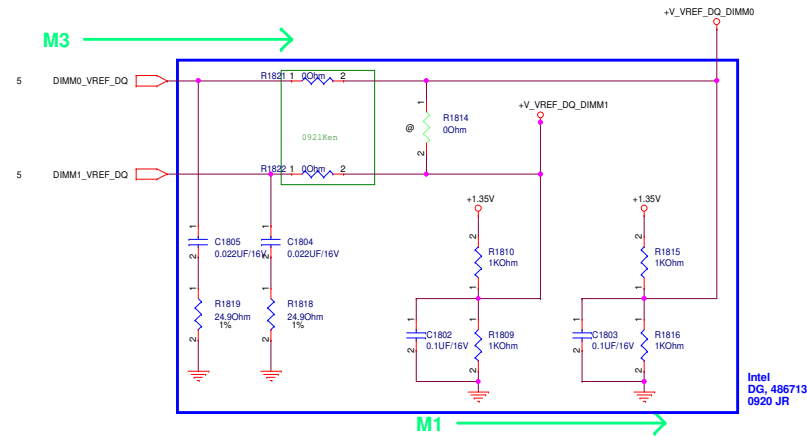
PEGATRON		Title : DDR3L(1)_SO-DIMM0	
BG1CORE		Engineer: Ruby Tsal	
Size Custom	Project Name PT10SG	Rev 1.1	
Date: Tuesday, February 26, 2013		Sheet 16 of 104	



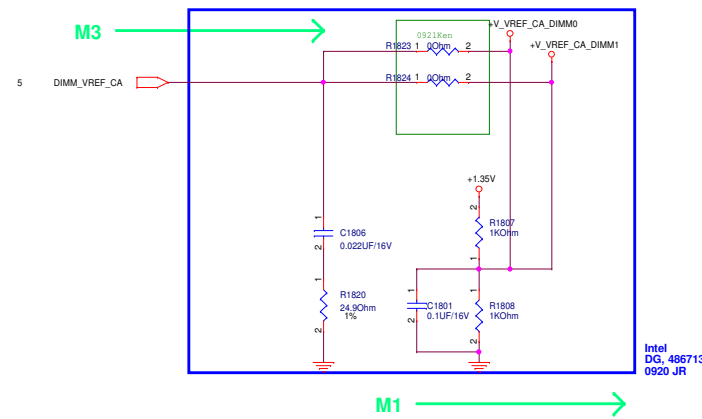
PEGATRON		Title : DDR3(2)_SO-DIMM1	
BG1CORE		Engineer: <i>Ruby Tsal</i>	
Size Custom	Project Name PT10SG	Rev 1.1	
Date: Tuesday, February 26, 2013	Sheet 17 of 104		

DDR3L Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

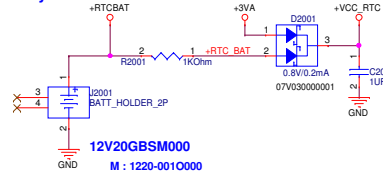


Intel 0203
M3+M1: Default Recommendation

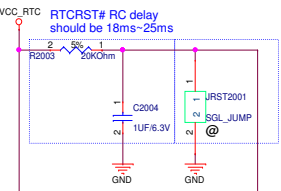


+1.35V		+1.35V	6,16,57,83
+V_VREF_DQ_DIMM0		+V_VREF_DQ_DIMM0	16
+V_VREF_CA_DIMM0		+V_VREF_CA_DIMM0	16,17
+V_VREF_DQ_DIMM1		+V_VREF_DQ_DIMM1	17
+V_VREF_CA_DIMM1		+V_VREF_CA_DIMM1	16,17

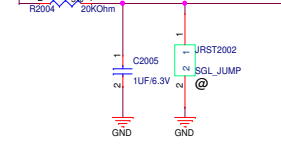
RTC battery



+VCC_RTC	→ +VCC_RTC	22,27
+3VA	→ +3VA	27,30,33,57,60,65,81,88,93
+3VS	→ +3VS	4,16,17,21,22,23,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,91,92
+3VSUS_ORG	→ +3VSUS_ORG	21,22,24,25,26,27
+12VS	→ +12VS	28,48,57,91
+1.5VS	→ +1.5VS	21,22,24,26,27,53,57,84



TPM Settings	JRST2001
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)



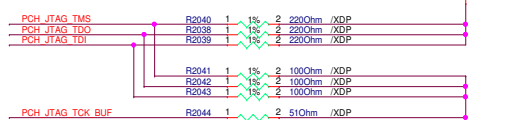
Request by CSC
for CMOS clear
function

CMOS Settings	JRST2002
Clear CMOS	Shunt
Keep CMOS	Open (Default)

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High: Enable Internal VRs



R1.0
For JTAG to pull high and low.



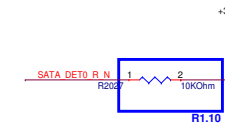
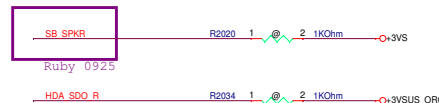
Strap information:

HDA_SPKR: No reboot strap
Low: Disable (Default)
High: Enable

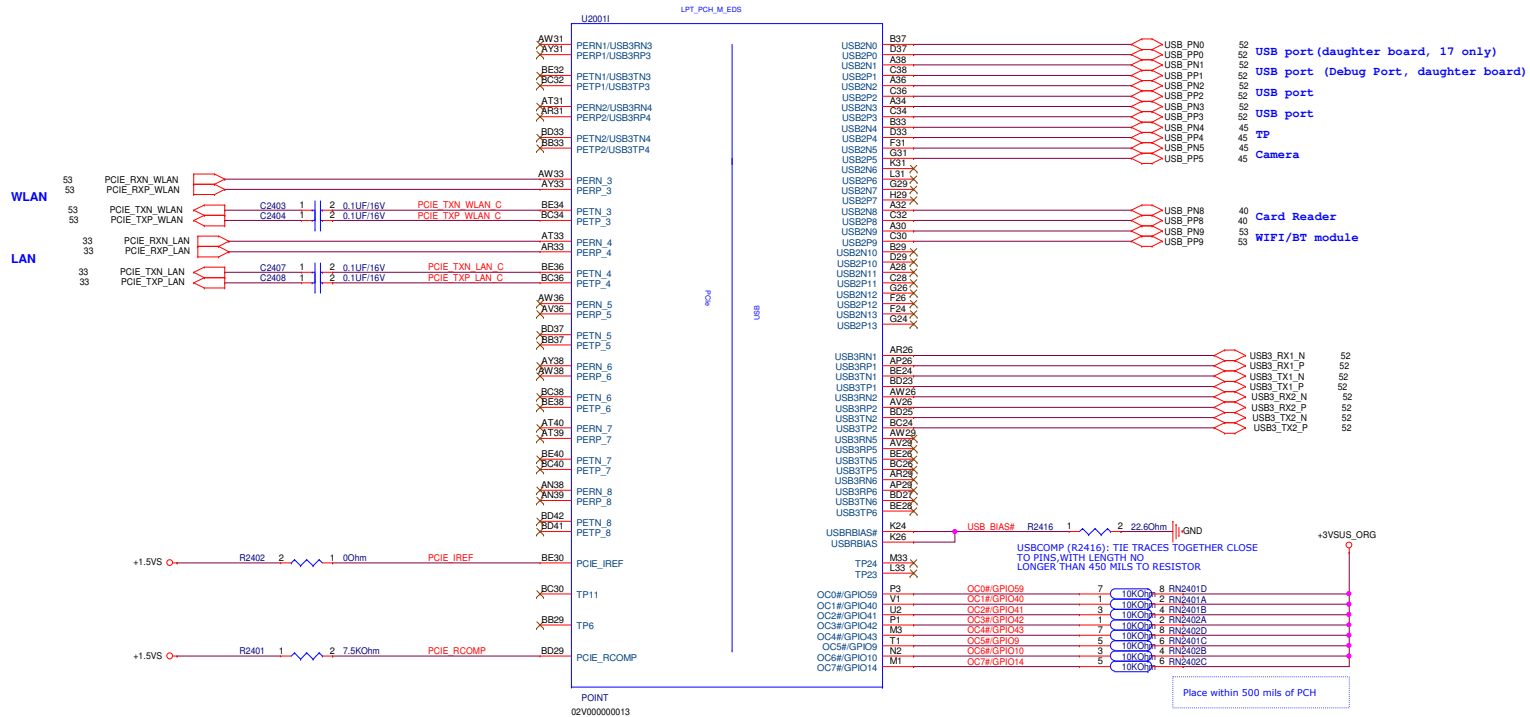
HDA_SDO:
1. Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2. HDA_SDO which sample high on the rising edge of PWROK
Will also disable Intel ME.

HDA_DOCK_EN#: Reserved

[0216]: ACZ_SYNC strap is no longer supported on LPT, by Intel FAE Stu.







+3VSUS +3VSUS 22,23,27,28,30,33,37,53,61,92

+3VSUS_ORG +3VSUS_ORG 20,21,22,25,26,27

+1.5VS +1.5VS 20,21,22,26,27,53,57,84



USB port (daughter board, 17 only)

USB port (Debug Port, daughter board)

USB port

USB port

TP

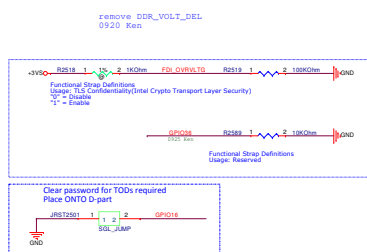
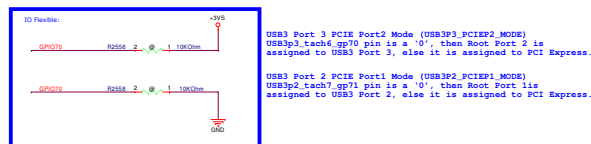
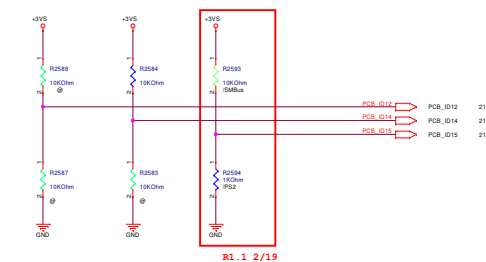
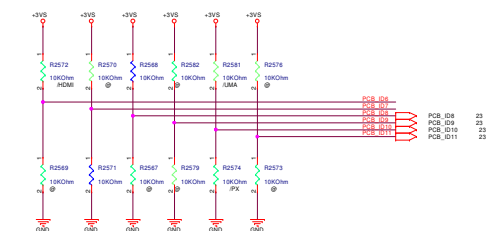
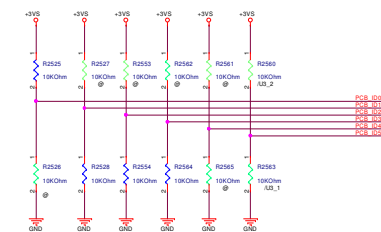
Camera

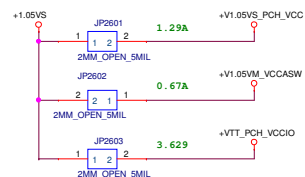
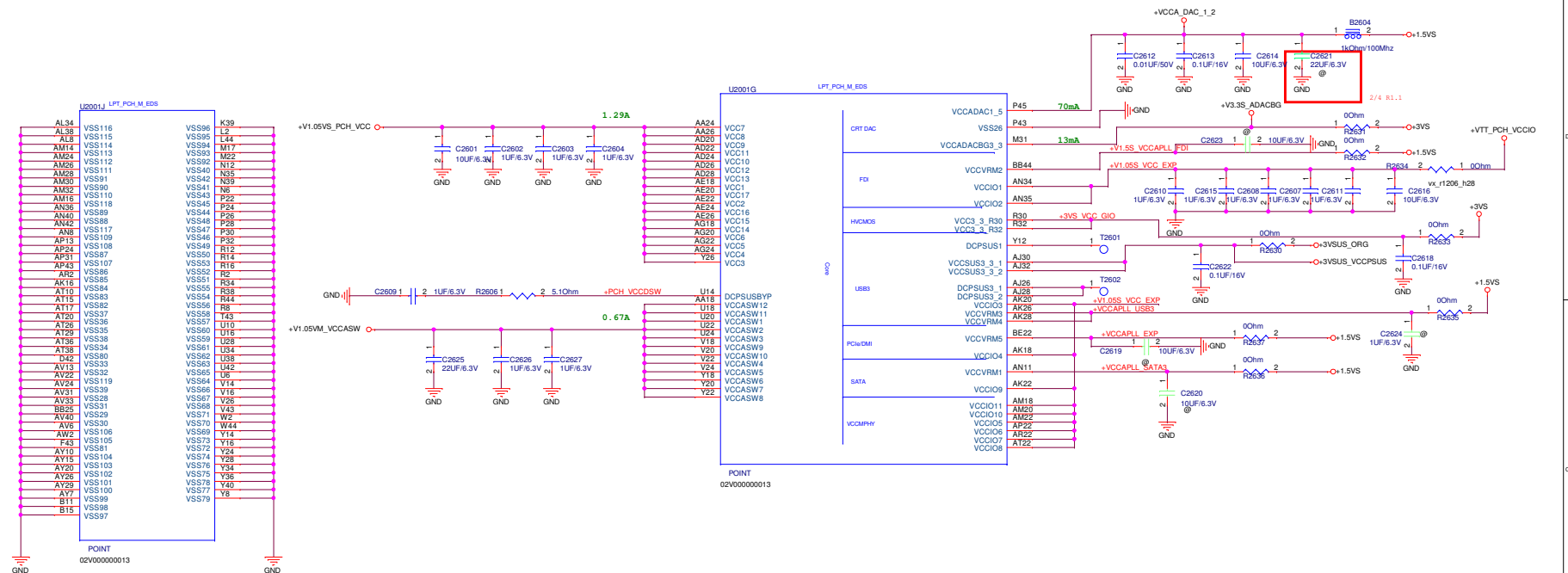
Card Reader

WIFI/BT module

ID0	ID1	ID2	PCB Rev.
0	0	0	R1.0
1	0	0	R1.1
0	1	0	R2.0
1	1	0	R2.1
0	0	1	TBD
1	0	1	TBD
0	1	1	TBD
1	1	1	TBD

ID7	ID8	CPU PWR.
0	0	CPU 17W
1	0	CPU 35W
0	1	CPU 45W
1	1	TBD

R1.1 2/19

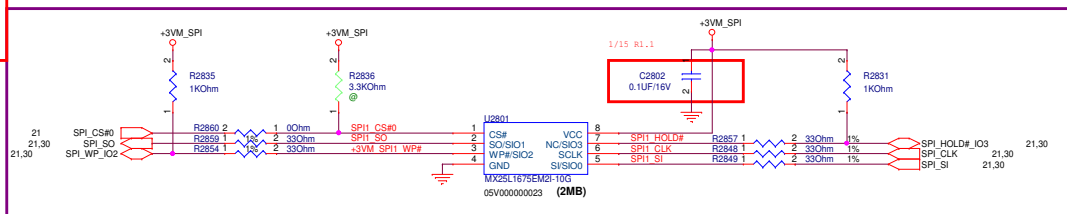
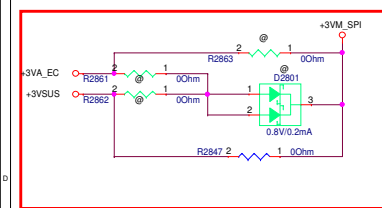


+V1.05VM_VCCASW	+	V1.05VM_VCCASW	27
+V1.05VS_PCH_VCC	+	V1.05VS_PCH_VCC	25
+VTT_PCH_VCCIO	+	VTT_PCH_VCCIO	27
+1.05VS	+	+1.05VS	4,27,32,57,80,82
+1.5VS	+	+1.5VS	20,21,22,24,27,53,57,84
+3VS	+	+3VS	4,16,17,20,21,22,23,25,27,28,30,31,32,36,40,45,46,48,50,51,53,57,91,92
+VCCA_DAC_1_2	+	VCCA_DAC_1_2	
+V3_3S_ADACBG	+	V3_3S_ADACBG	
+3VSUS_VCCPSUS	+	+3VSUS_VCCPSUS	27



PEGATRON		Title : PCH(8)_POWER_GND	
BG11CORE		Engineer: Ruby Tsal	
Size Custom	Project Name PT10SG	Rev 1.1	
Date: Tuesday, February 26, 2013	Sheet 27 of 104		

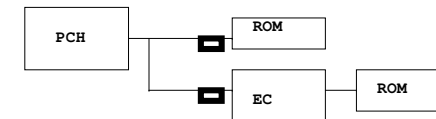
PCH SPI ROM



For QUAD I/O
Ruby 0928 update

+3VS	4,16,17,20,21,22,23,25,26,27,30,31,32,36,40,45,46,48,50,51,53,57,91,92
+12VS	48,57,91
+12VSUS	33,51,81,91
+3VM_SPI	27
+3VSUS	22,23,27,30,33,37,53,81,92

	16Mb	32Mb
QUAD	05V000000023	05V000000022
DUAL	05V000000010	05V000000005

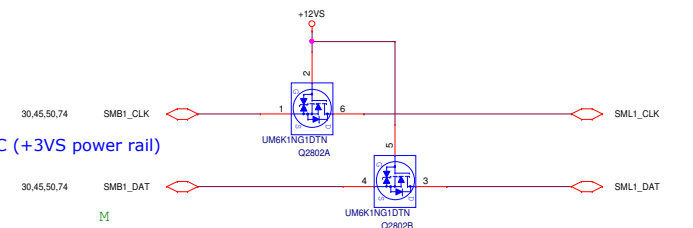


change DP to LVDS SMBus
to SCL_3A, SDA_3A
JR 0924

SMB1 Link device (+3VS)
DGPU Thermal sensor
RTD2132R(eDP to LVDS)

EC (+3VS power rail)

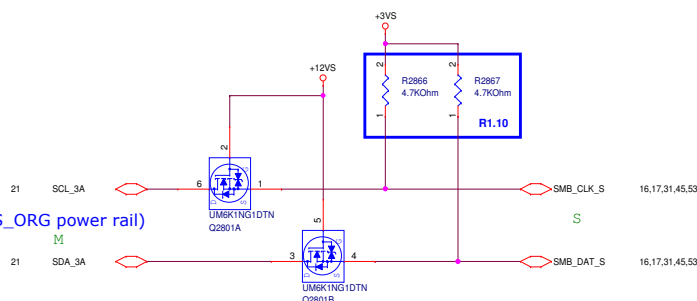
PCH(+3VSUS_ORG power rail)



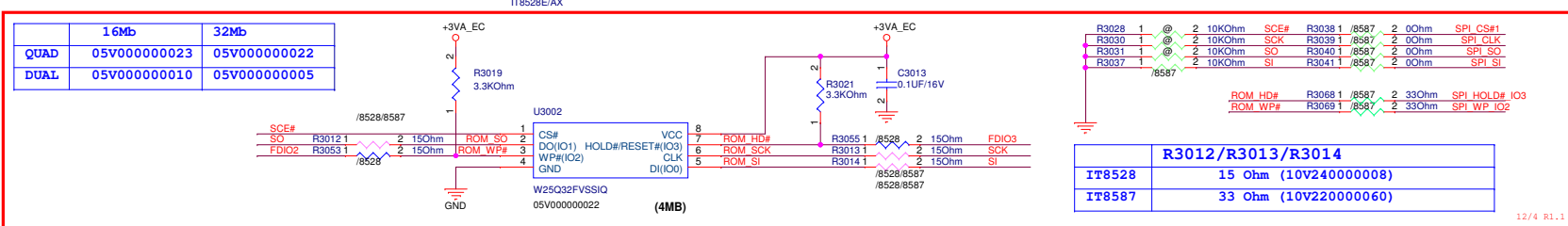
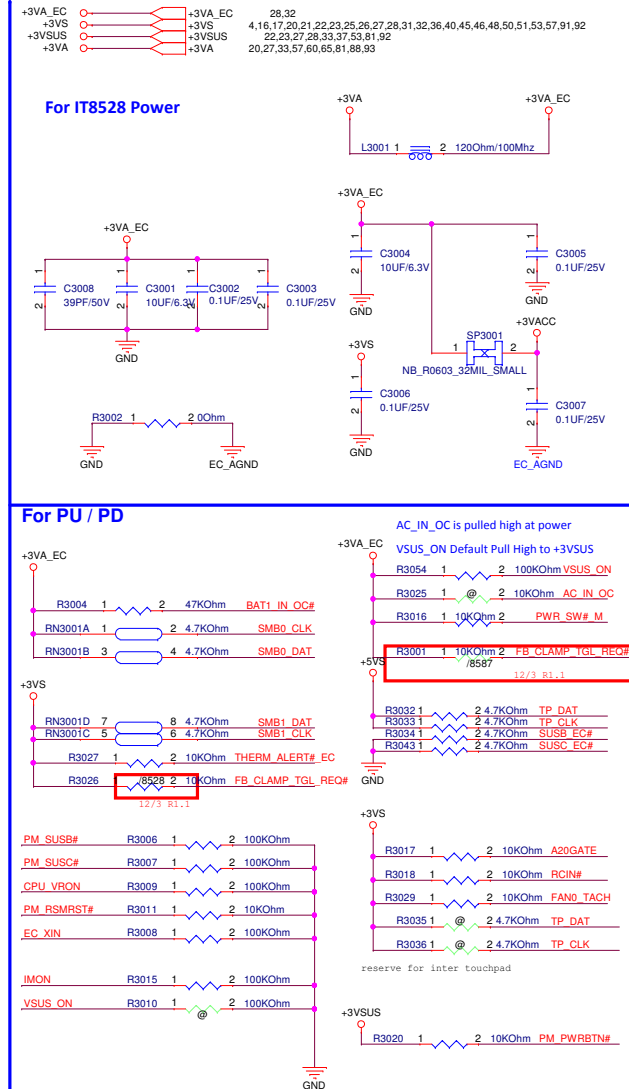
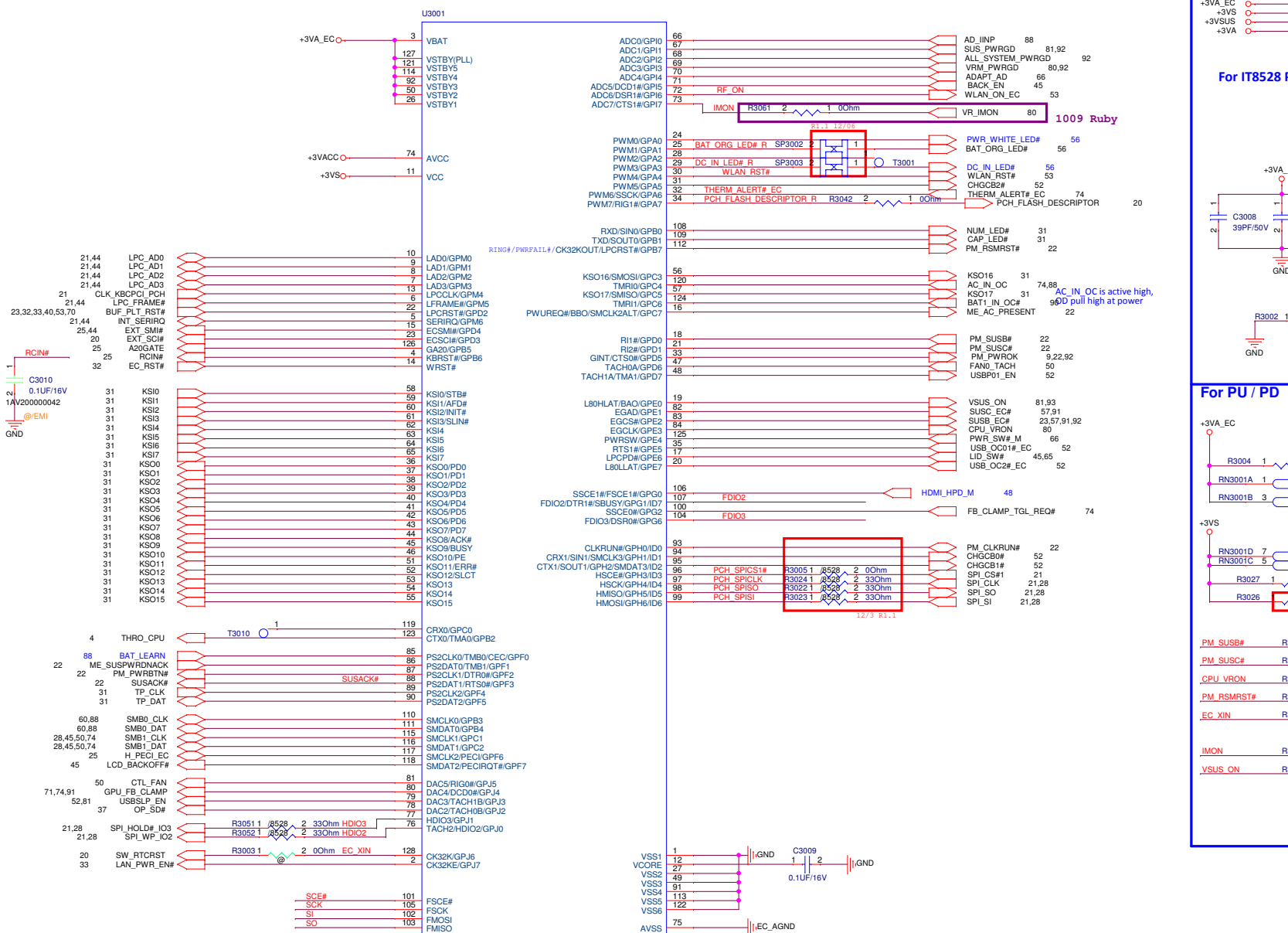
remove
JR 0924

PCH(+3VSUS_ORG power rail)

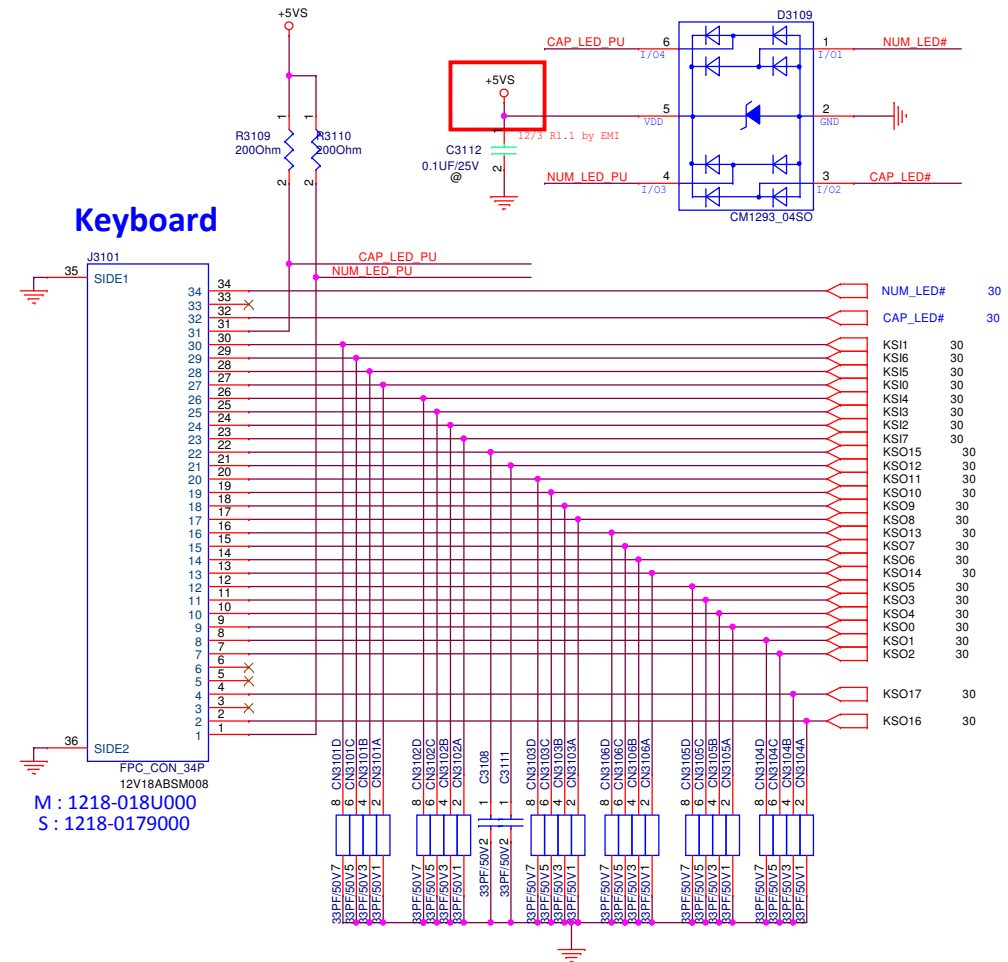
SMBUS Link device (+3VS)
SPD (A0h,A4h)
WUAV (NC)
Touch Pad
RTD2132R(eDP to LVDS) (6Ah)



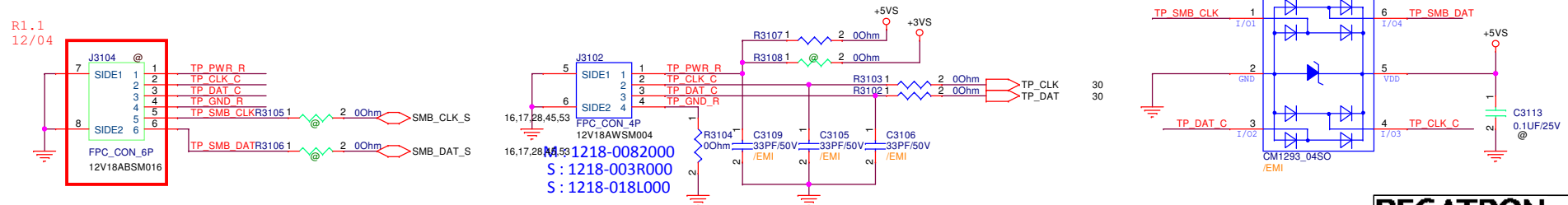
<http://forum.hocvienit.vn>



KB CONNECTER FOR 15"



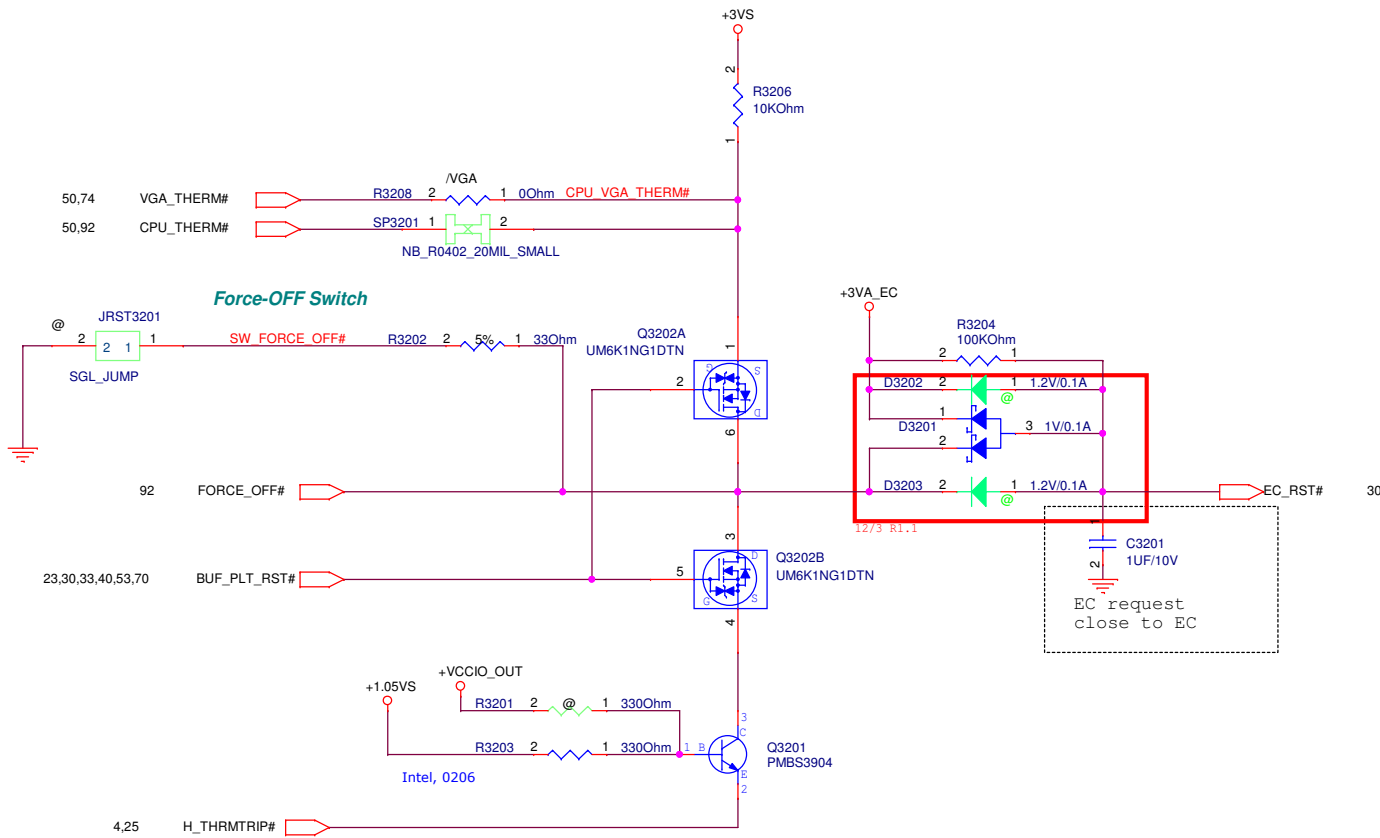
Touch Pad Module



<http://forum.hocvienit.vn>

Thermal Policy

+3VA_EC 28,30
+3VS 4,16,17,20,21,22,23,25,26,27,28,30,31,36,40,45,46,48,50,51,53,57,91,92

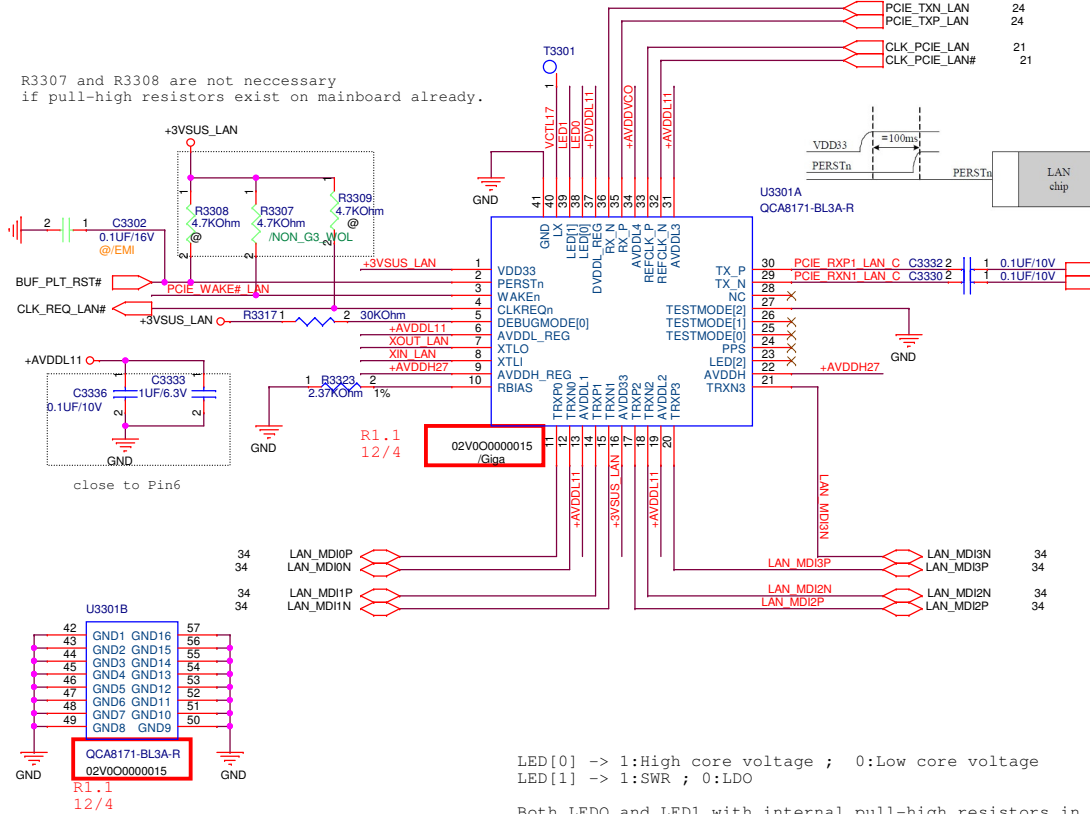


PEGATRON		Title : RST_Reset Circuit	
BG1CORE		Engineer: Ruby Tsai	
Size B	Project Name PT10SG		Rev 1.1
Date: Tuesday, February 26, 2013		Sheet	32 of 104

ATHEROS/QCA8171(gigaLAN)	02V000000015
ATHEROS/QCA8172(100LAN)	02V000000016

3.3V Current/Power	QCA8171	QCA8172
LDO mode	277mA/915mW	111mA/366mW
SWR mode	136mA/448 mW	56mA/183mW

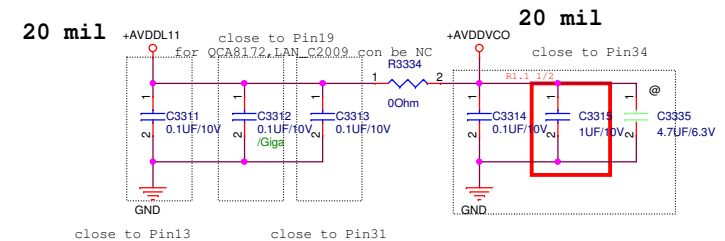
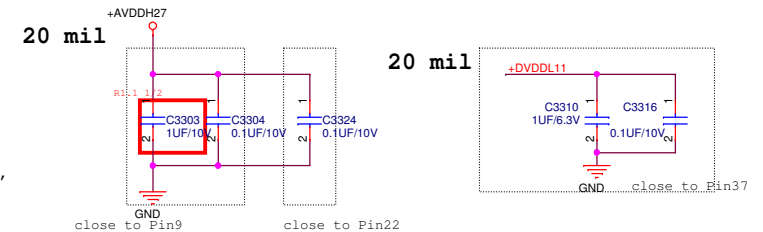
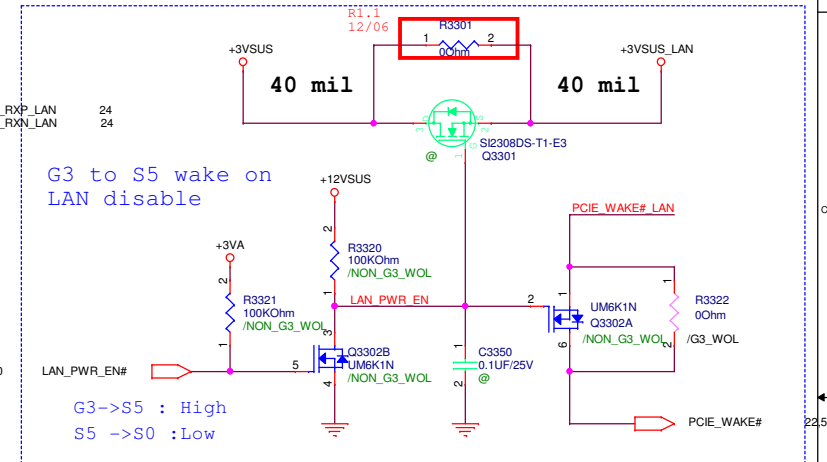
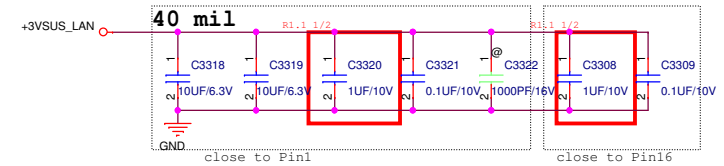
R3307 and R3308 are not necessary if pull-high resistors exist on mainboard already.

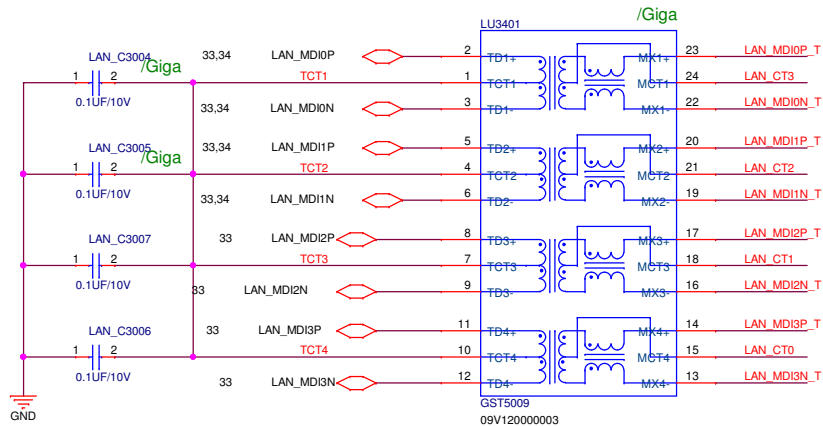


LED[0] -> 1:High core voltage ; 0:Low core voltage
LED[1] -> 1:SWR ; 0:LDO

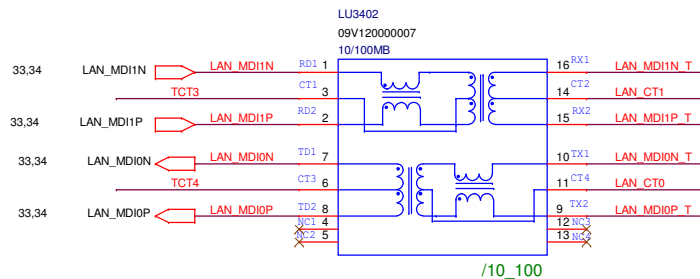
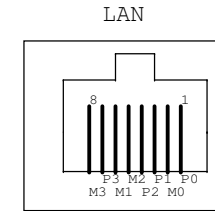
Both LED0 and LED1 with internal pull-high resistors in the chip, R3328, R3330, R3331 and R3332 must be removed.

For QCA8171-C, it can only work at high core voltage mode

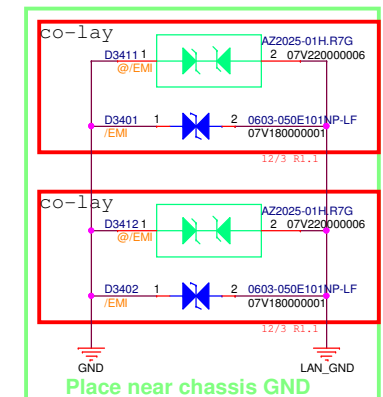
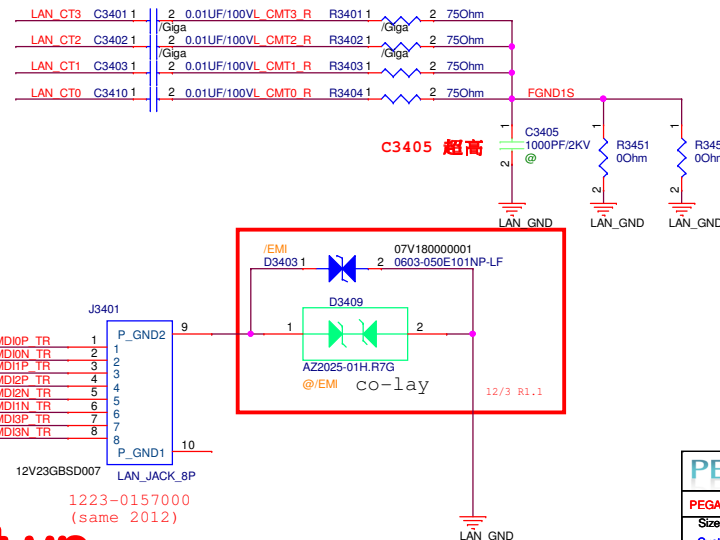
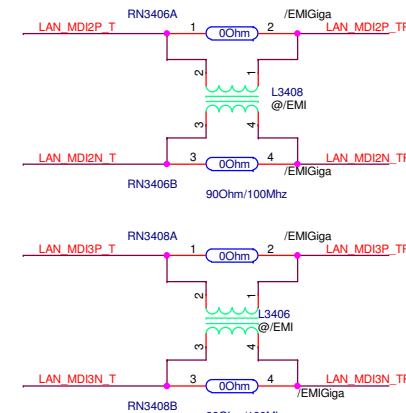
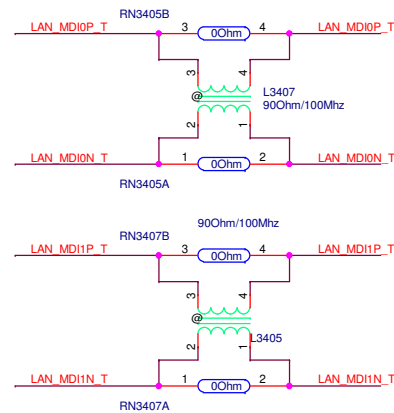
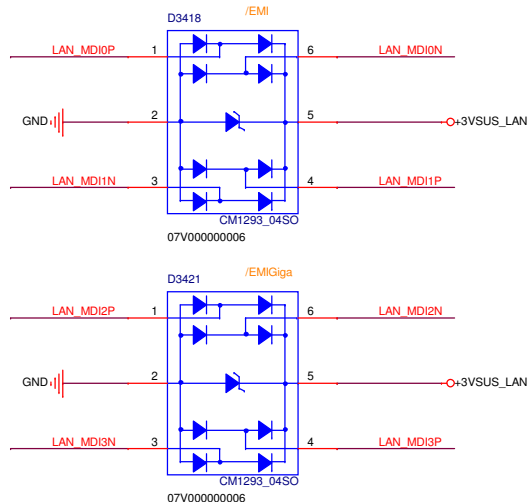




Transformer close J3401 1G



Transformer close J3401 10M/100M



Intel 1.01 Design Guide update #440484
R1.3 use dual mosfet



Resistor	SENSE_A
39.2K	PORT A
20.0K	PORT B
10.0K	Port C
5.11K	SPDIFOUT
2.49K	Pull-up to AVDD

Table 3. Jack Detect

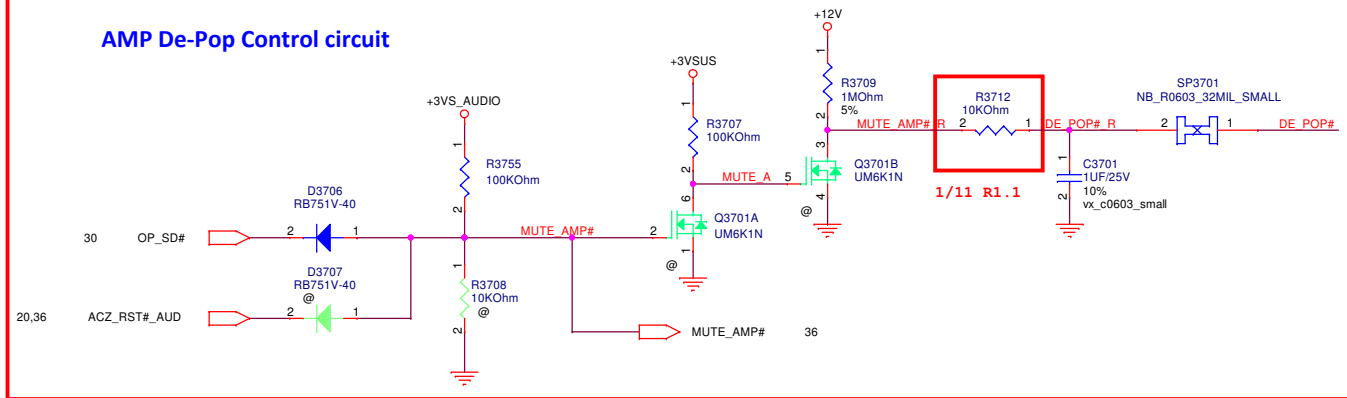
Pins 40-QFN	Port	Input	Output	Headphone	BTL	Mic Bias (Vref pin)	Input boost amp
22/23	A		Yes	Yes			
17/18	B	Yes				Yes	Yes
14/15	C	Yes				Yes	Yes
32/33/36/37	D		Yes		Yes		
3 (CLK=2)	E (DMIC0)	Yes				NA	Yes
4 (CLK=2)	F (DMIC1)	Yes				NA	Yes
40	SPDIF_OUT		Yes				

Table 1. Port Functionality

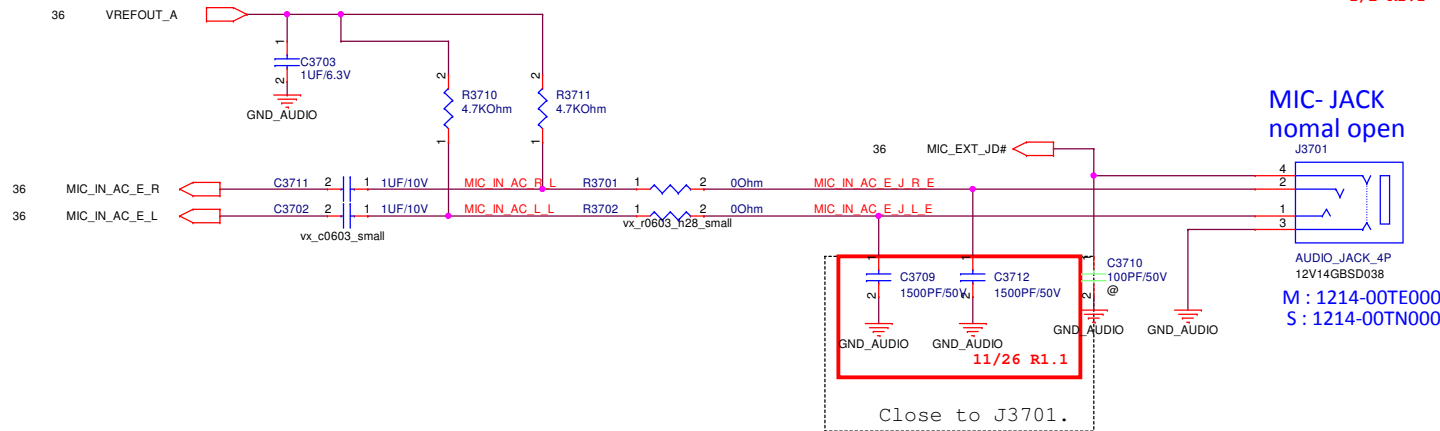
PEGATRON Title : AUD(1)_92HD95

BU1-RD Div.3-HW RD Dept.1		Engineer:	
Size C	Project Name	Rev 1.1	
Date: Tuesday, February 26, 2013		Sheet	36 of 99

AMP De-Pop Control circuit

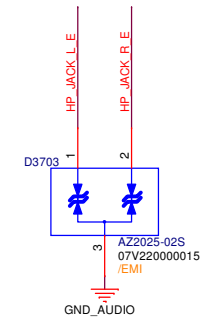
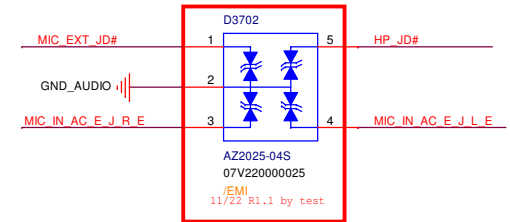


1/2 R1.1



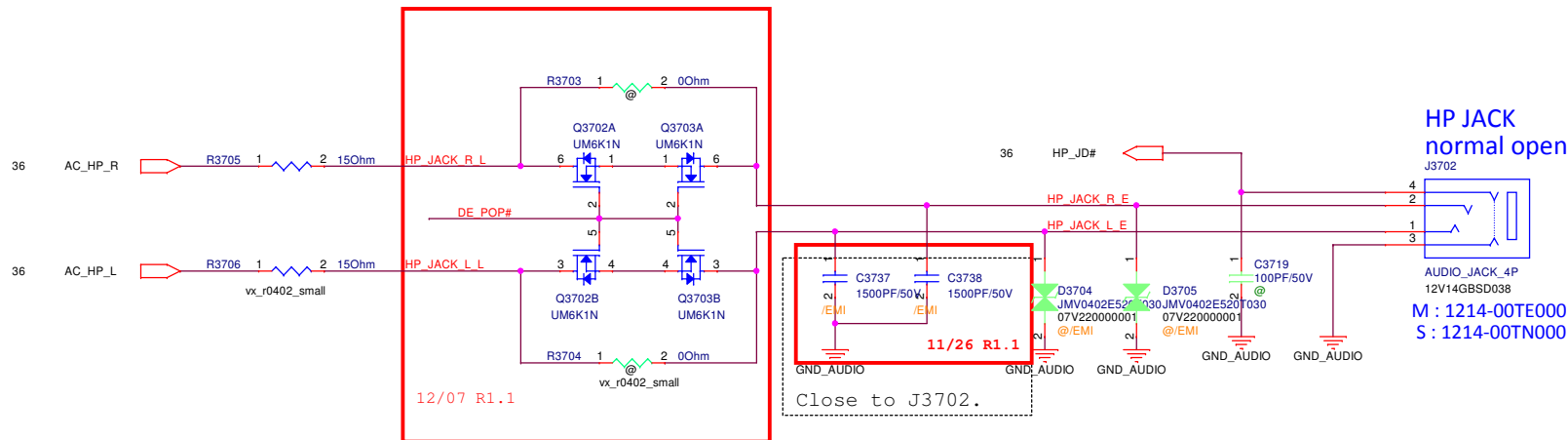
MIC- JACK
normal open

M : 1214-00TE000
S : 1214-00TN000



HP JACK
normal open

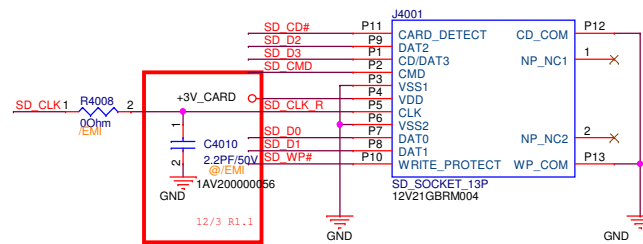
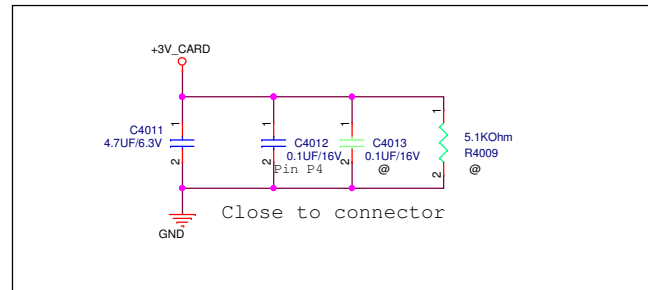
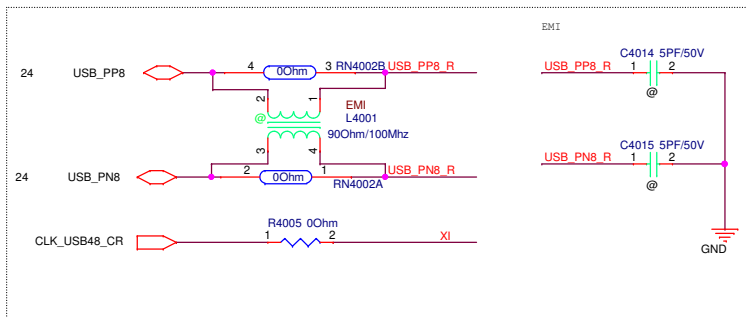
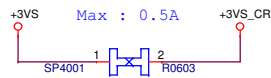
M : 1214-00TE000
S : 1214-00TN000



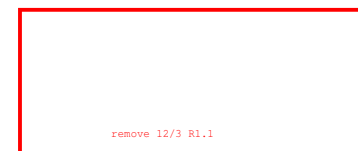
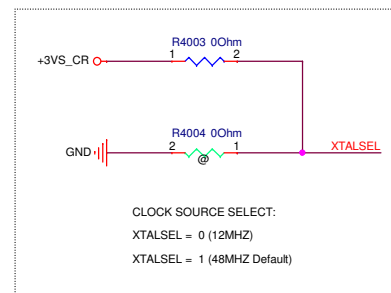
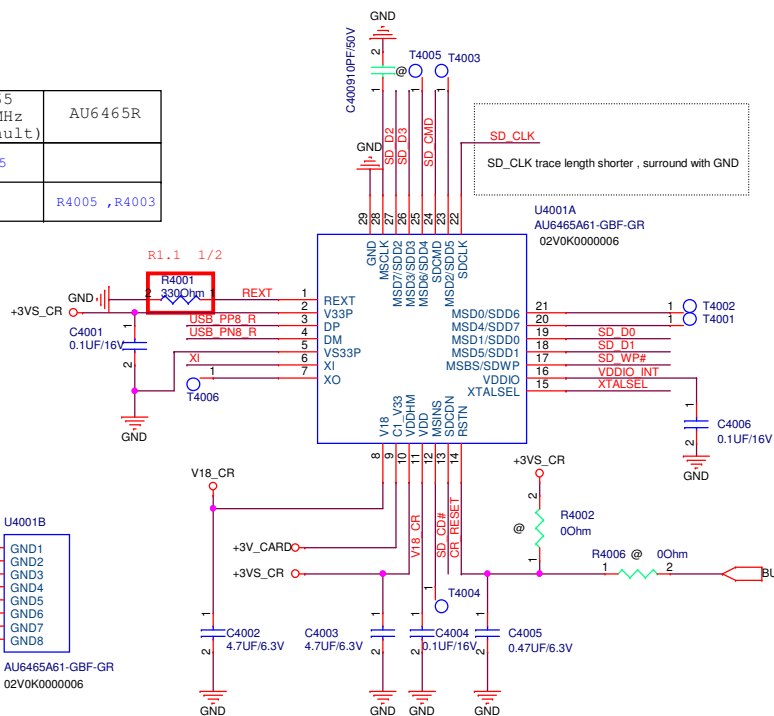
12/07 R1.1

11/26 R1.1

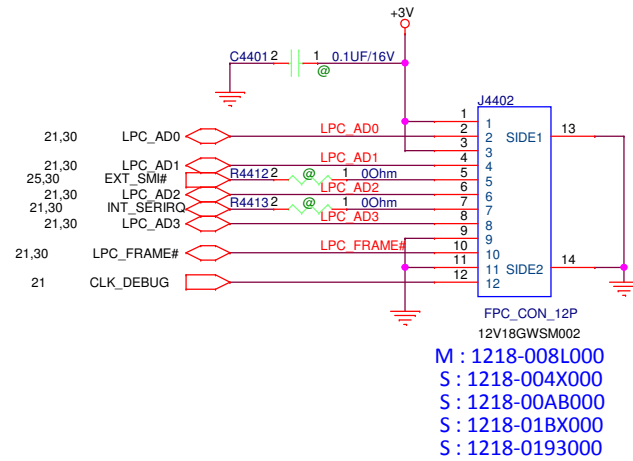
<http://forum.hocvienit.vn>



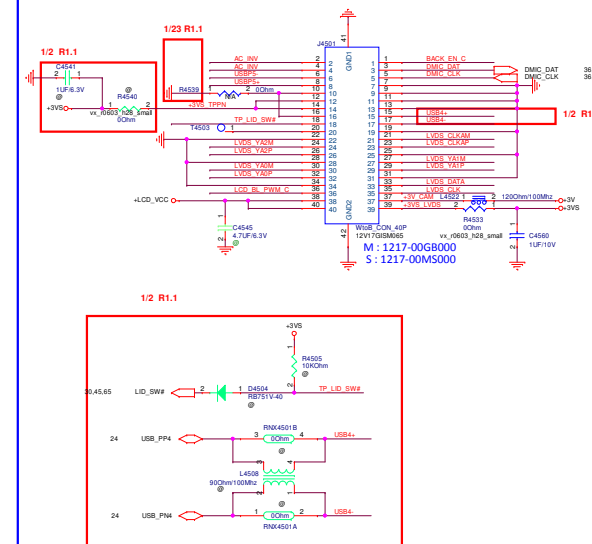
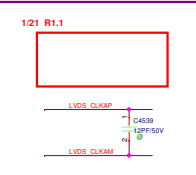
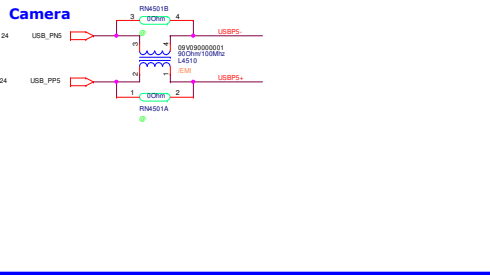
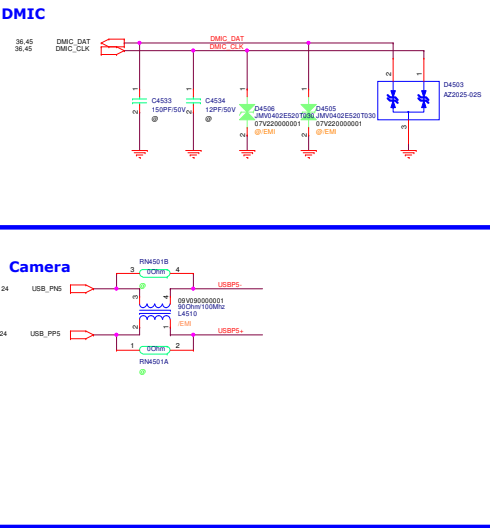
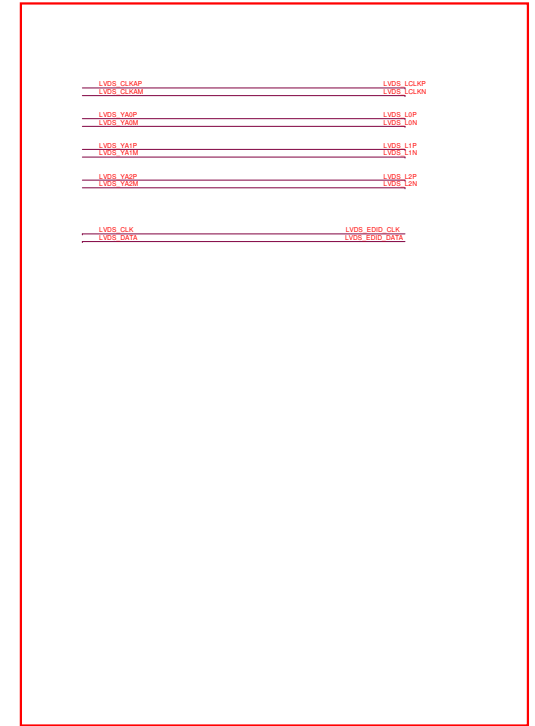
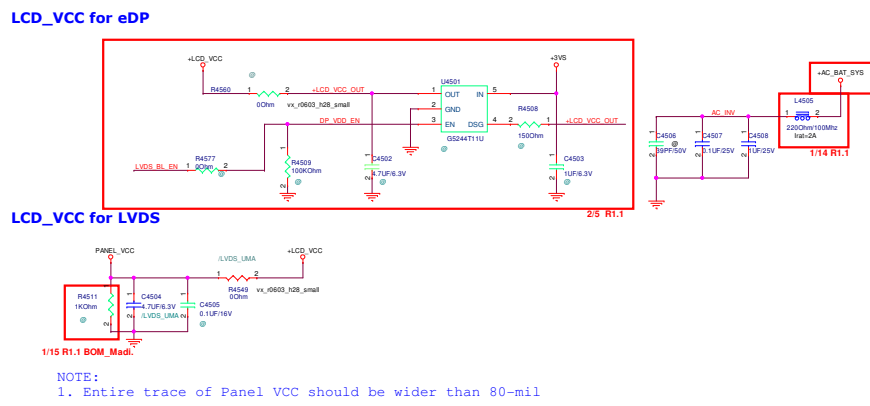
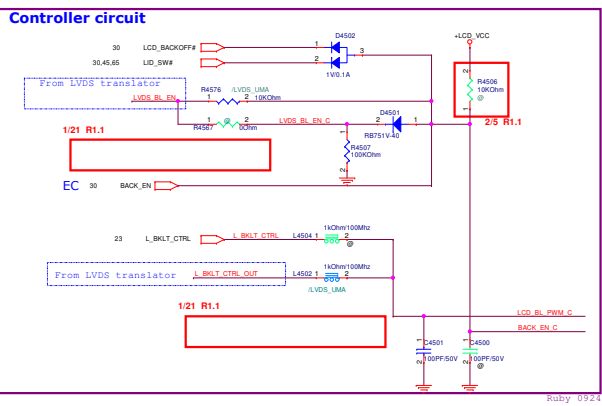
	AU6465 W/48MHz (Default)	AU6465R
Mount	R4005	
Unmount		R4005 ,R4003



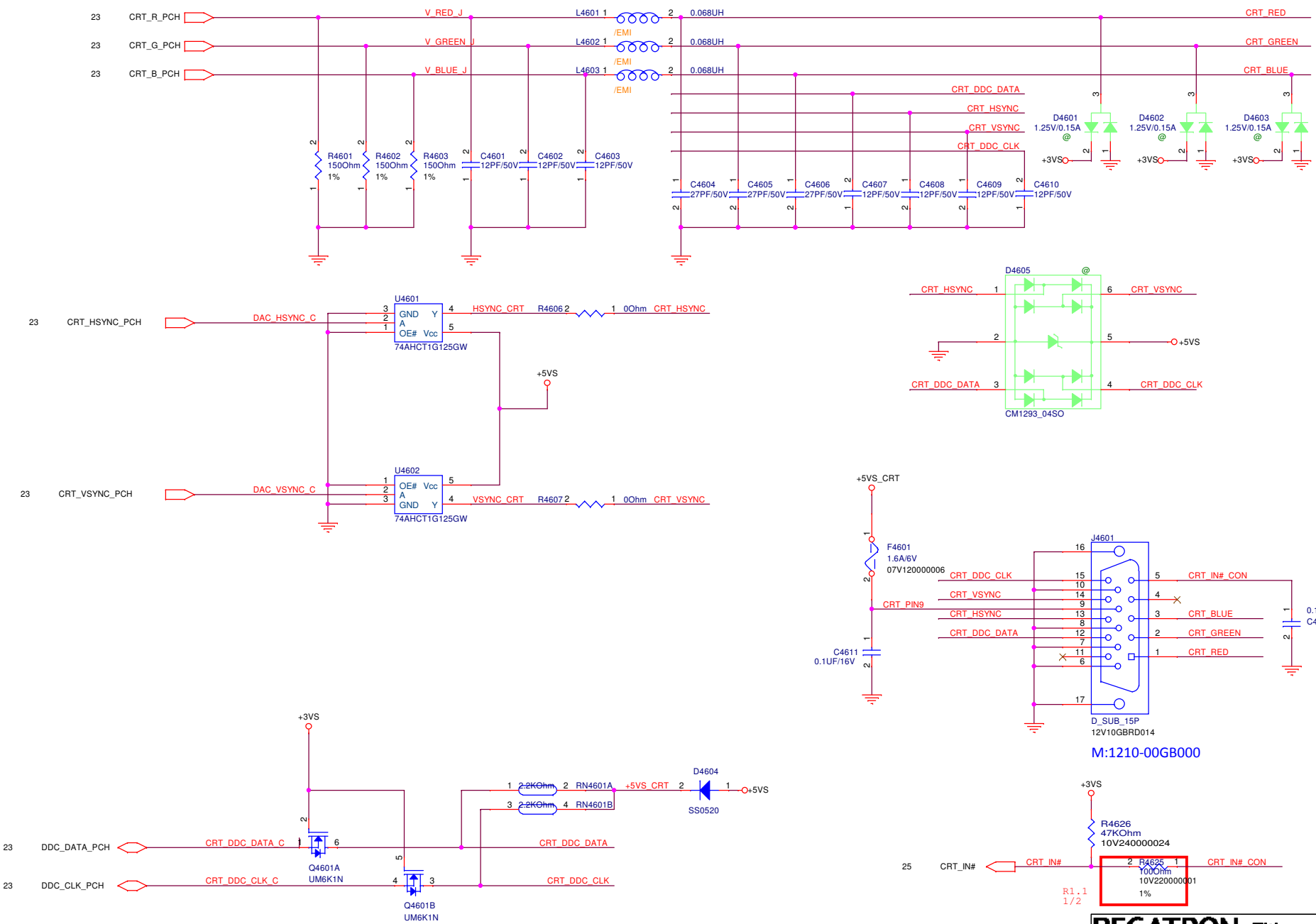
DEBUG CARD CONN.



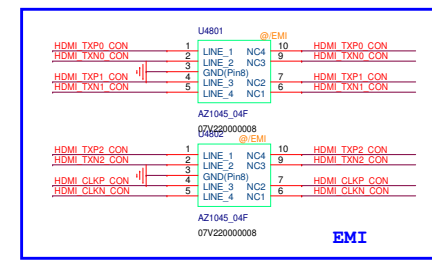
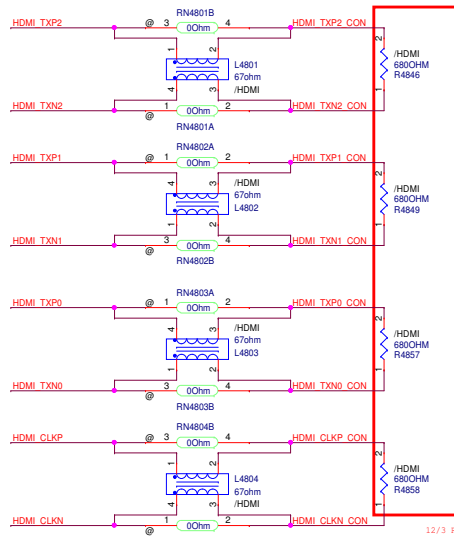
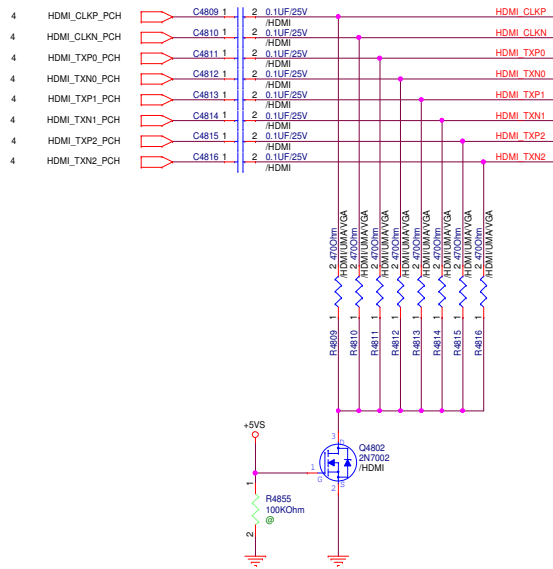
PEGATRON		Title : BUG_Debug	
BG1-CSC-HW R&D Dept.5		Engineer: Ruby Tsai	
Size B	Project Name PT10SG		Rev 1.1
Date: Tuesday, February 26, 2013		Sheet 44 of 104	



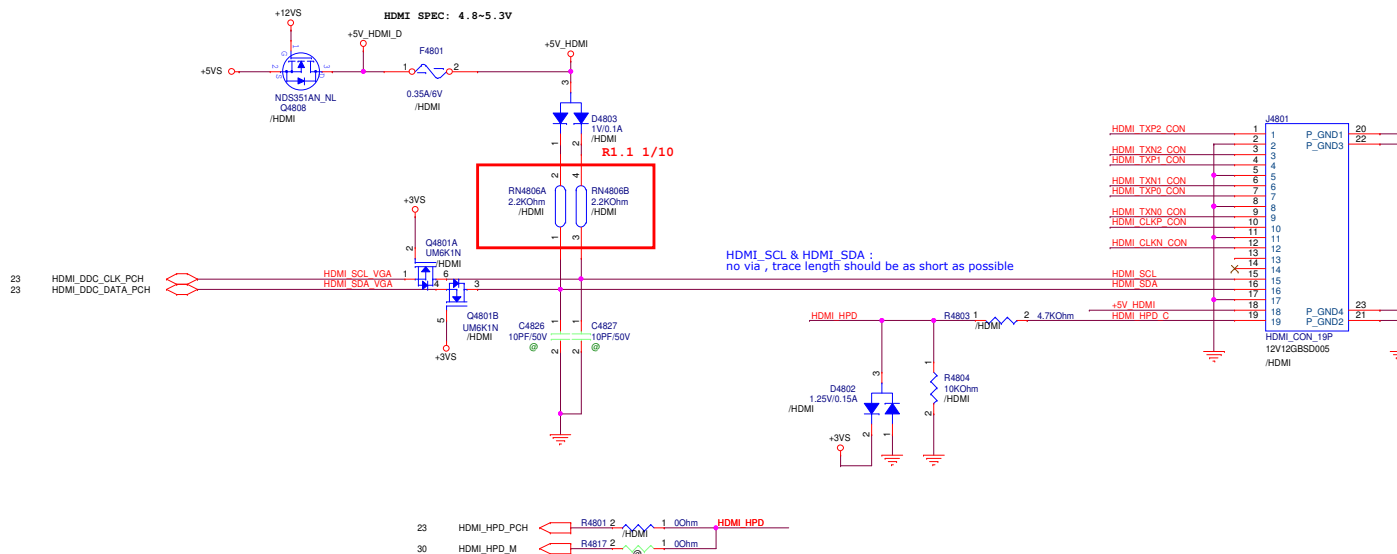
<http://forum.hocvienit.vn>



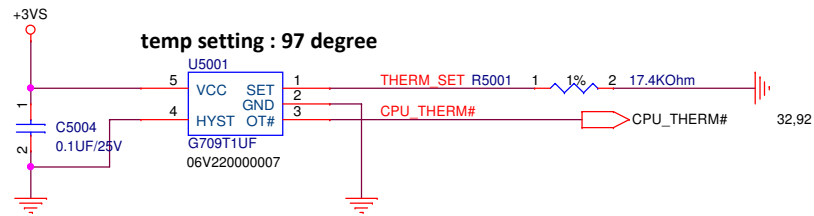
<http://forum.hocvienit.vn>



EMI

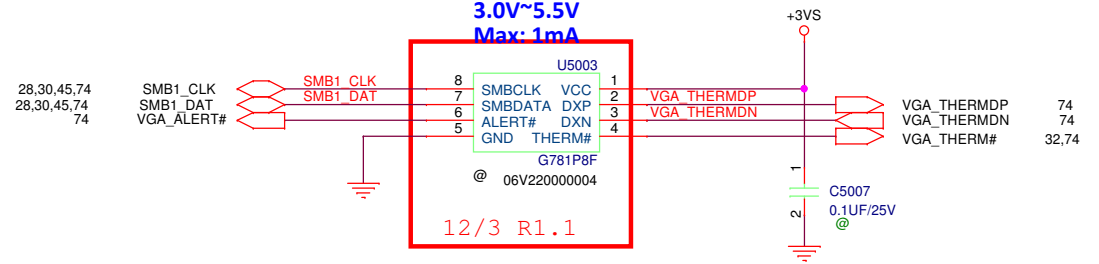


U5001 Close to CPU

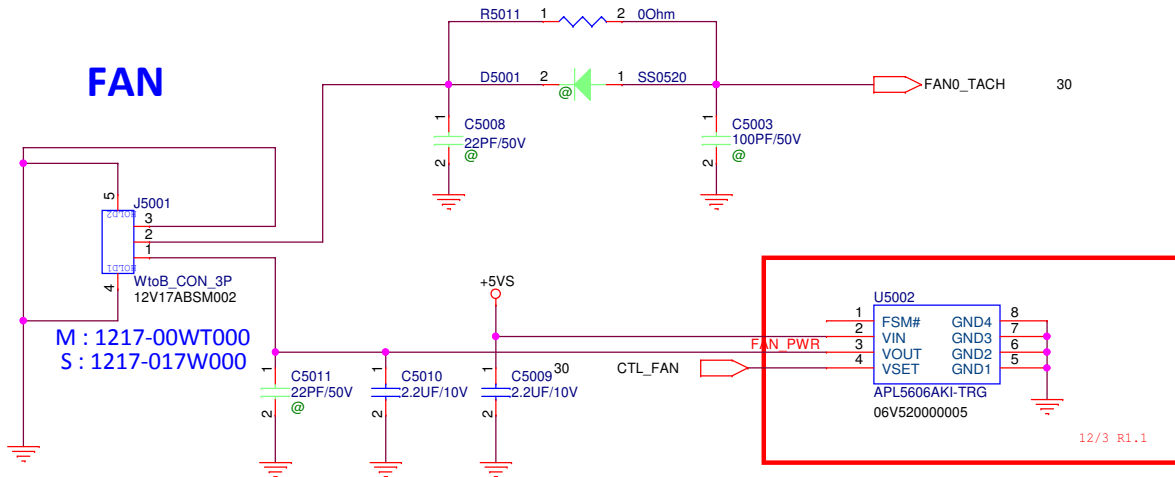


U5003 Close to GPU

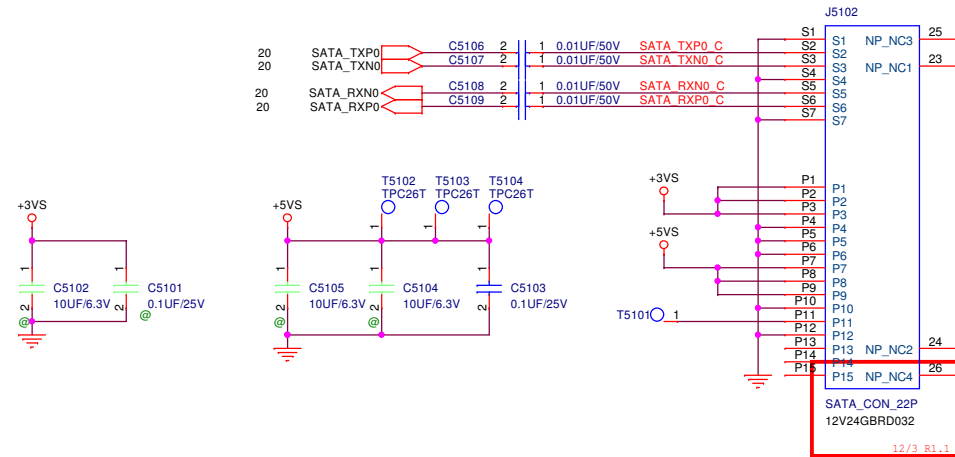
3.0V~5.5V
Max: 1mA



FAN



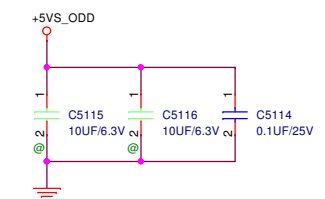
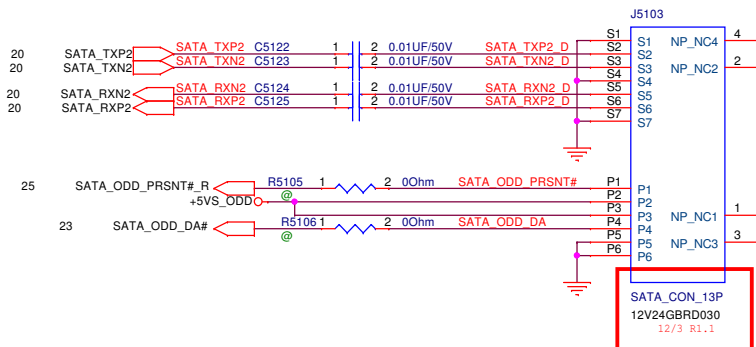
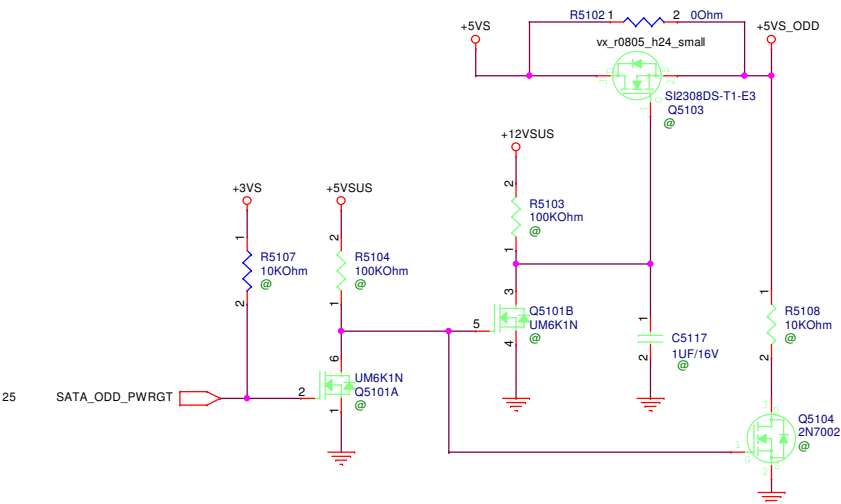
HDD



+5VS and +5VS_ODD Trace need more width to avoid blue Ray DVD rush current

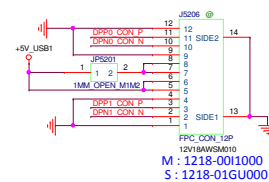
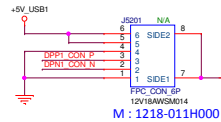
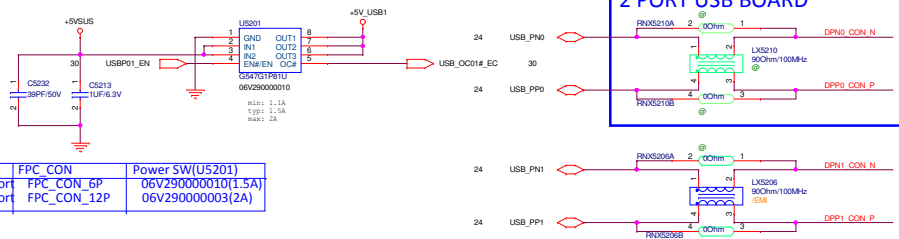
ODD

ZERO POWER ODD SUPPORT support Hokey turn off ODD power

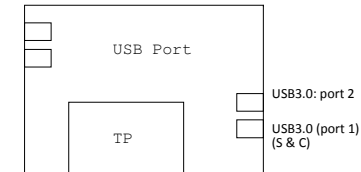


<http://forum.hocvienit.vn>

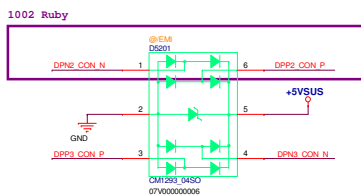
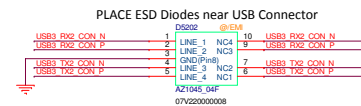
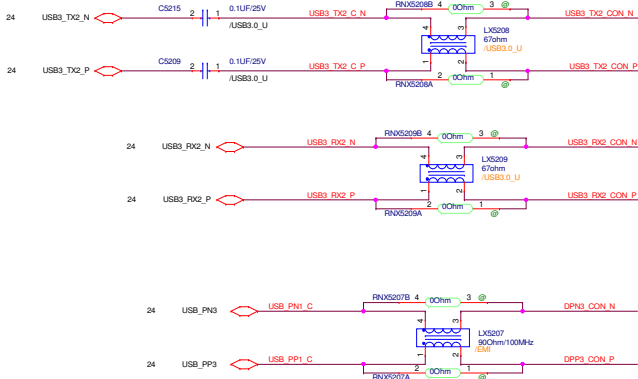
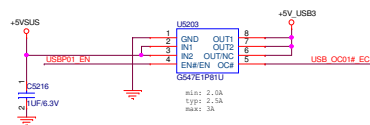
USB 2.0 port x2 (Left Up)



For 2port USB Board



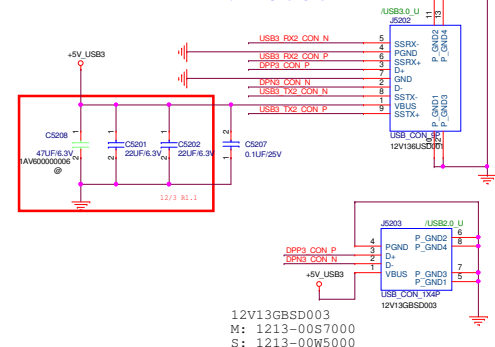
USB 3.0 ports x 1 (Right Up)



USBSLP / NON_USBSLP



vp/n:TBD
M: 1213-015K01B



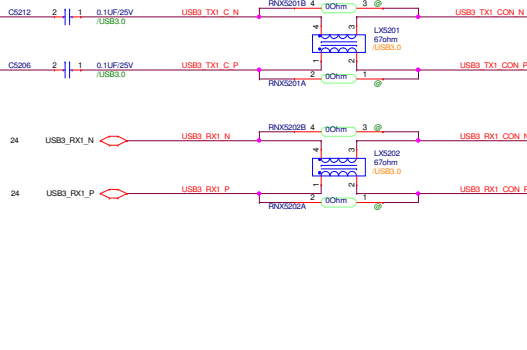
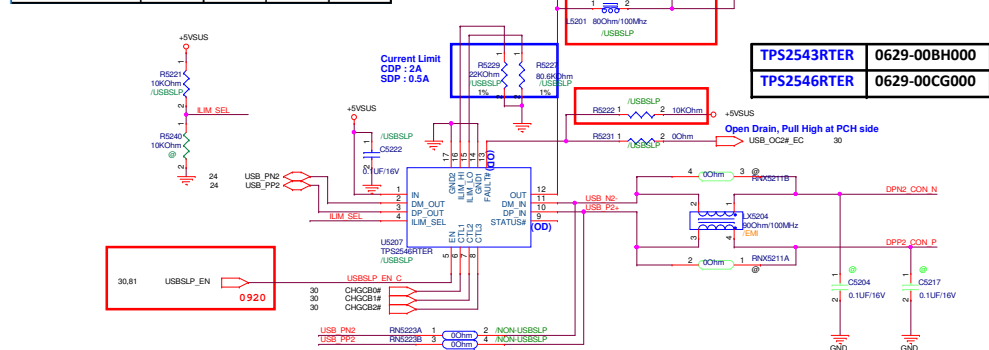
USB 3.0 ports x 1 with Sleep & Charge (Right Down)

Standard --> TPS2546RTER

Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	1	1	X
	0	0	1	X

Tod's spec

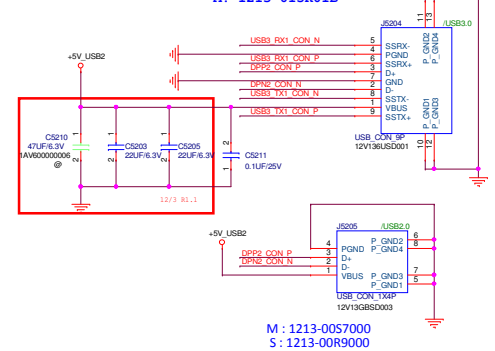
Battery Charge mode	
Apple 1.0A mode	Yes
DCP mode	Yes
Apple 2.0A mode	Yes



PLACE ESD Diodes near USB Connector



vp/n:TBD
M: 1213-015K01B

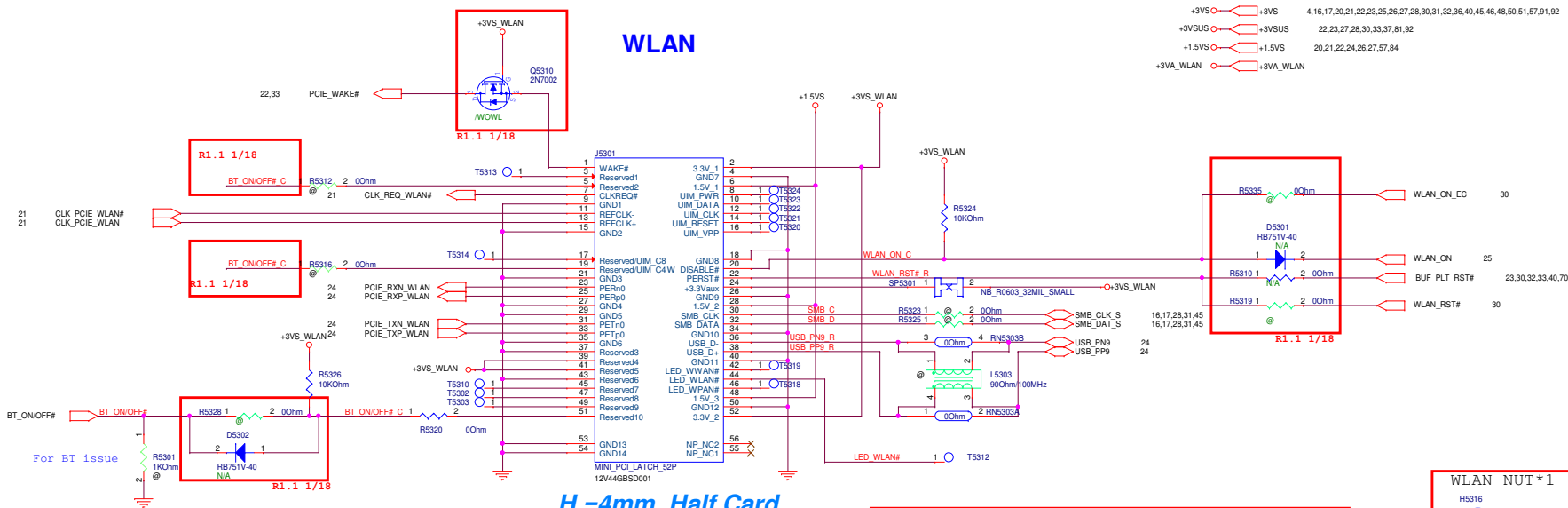


M: 1213-0057000
S: 1213-00R9000

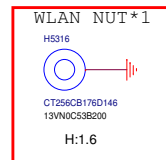
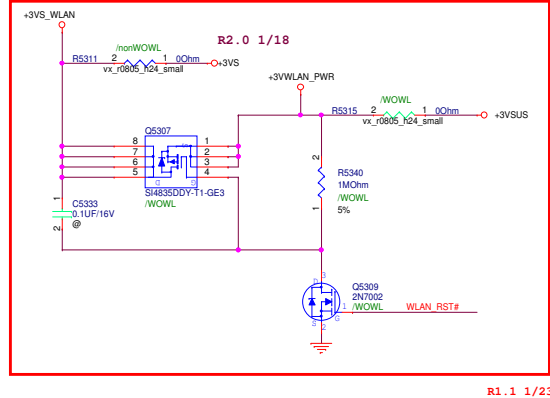
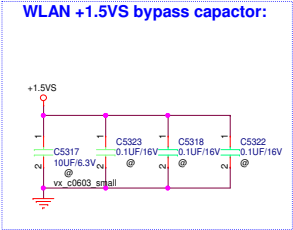
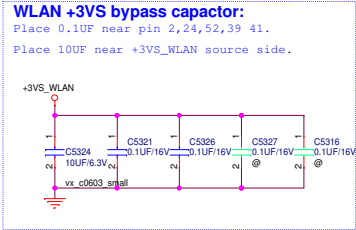
PEGATRON Title : USB JACK				
Rev	Project Name	Engineer: Ruby Tsai	Rev	1.1
Size	Control	PT10SG	Rev	1.1
WPC	Friday, February 26, 2010	Sheet	52	of 104

<http://forum.hocvienit.vn>

WLAN



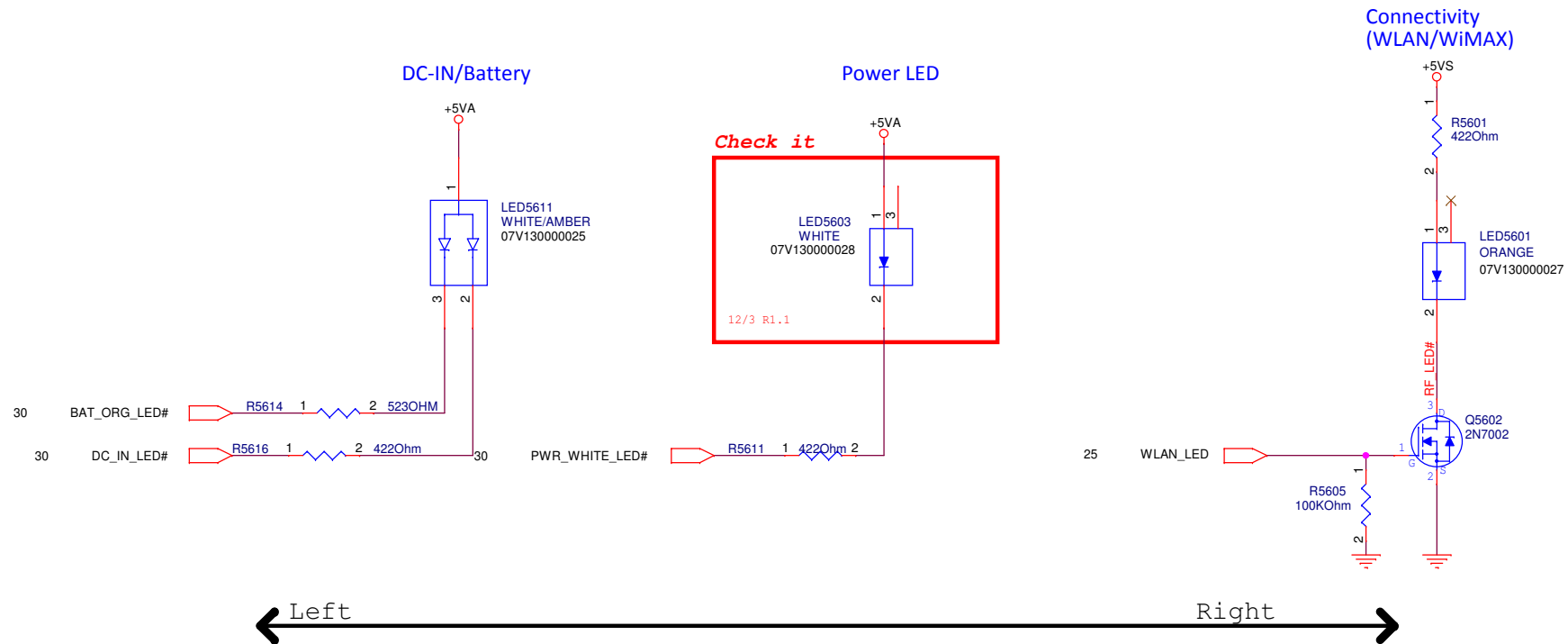
H=4mm Half Card

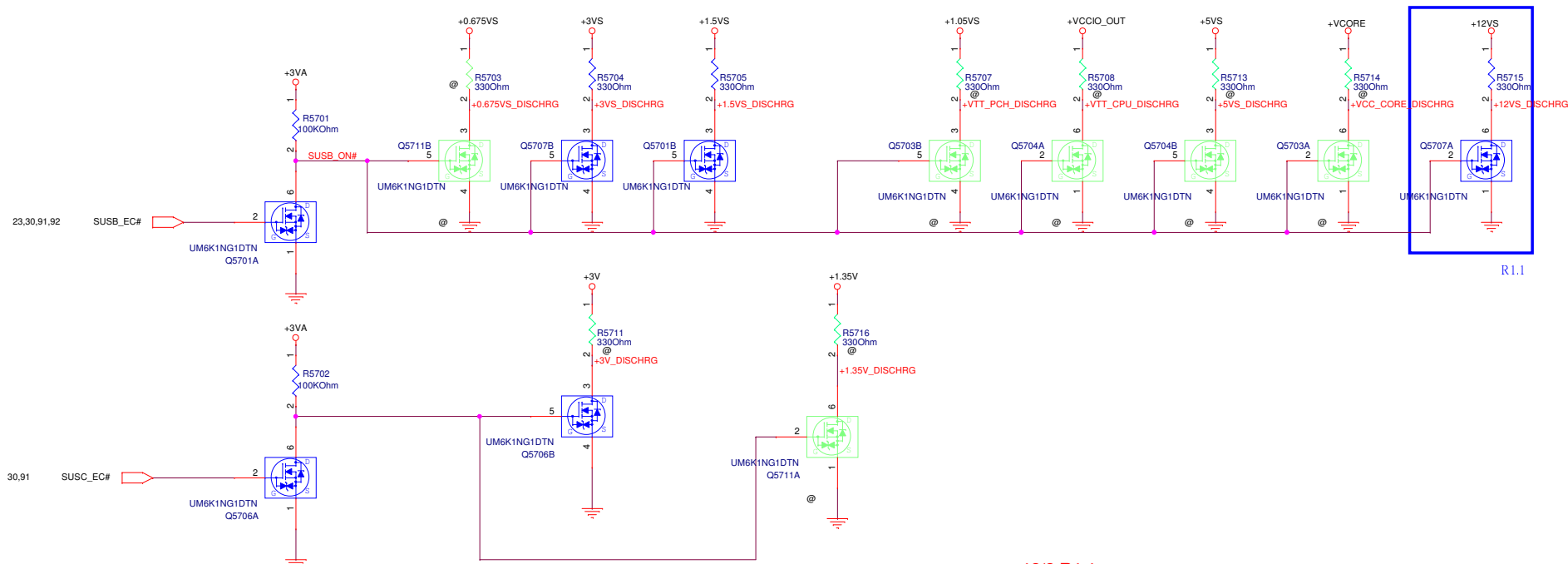


R1.1 1/23

<http://forum.hocvienit.vn>

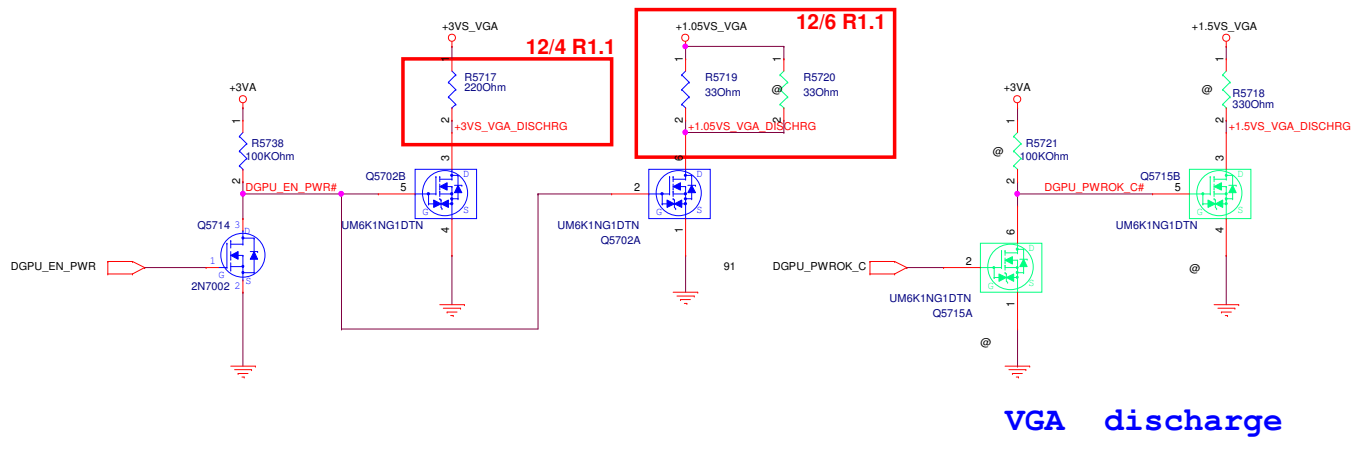
Order of Indicator LEDs DC-IN/Battery Power WiFi





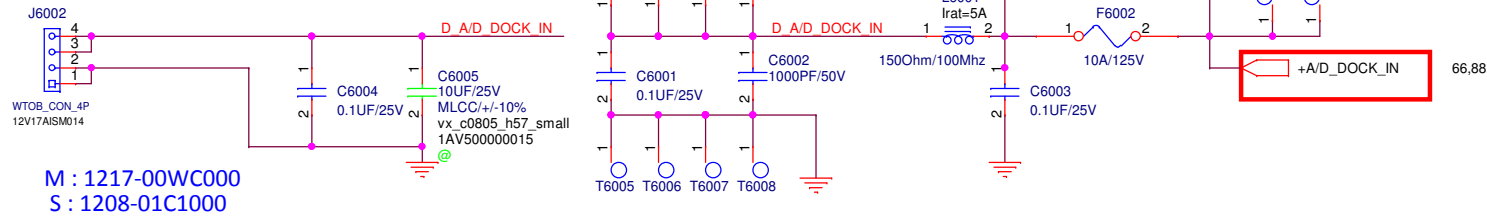
12/3 R1.1

+3VA	+3VA	20,27,30,33,60,65,81,88,93
+VCCORE	+VCCORE	6,9,80
+VCCIO_OUT	+VCCIO_OUT	4,6,32
+0.675VS	+0.675VS	16,17,83
+1.05VS	+1.05VS	4,26,27,32,80,82
+1.5VS	+1.5VS	20,21,22,24,26,27,53,84
+3VS	+3VS	4,16,17,20,21,22,23,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,91,92
+5VS	+5VS	30,31,36,46,48,50,51,56,66,80,87,91
+3V	+3V	23,44,45,91
+5V	+5V	91

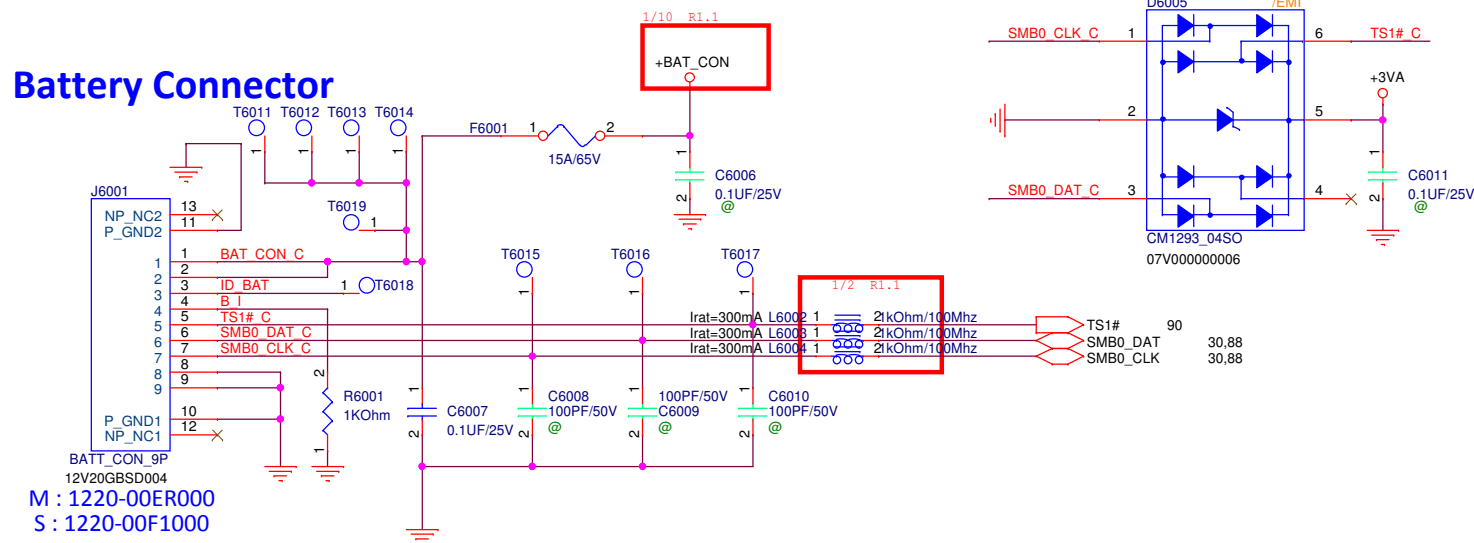


PEGATRON		Title : DSG Discharge	
BG1C0RE		Engineer: Ruby Tsal	
Size	Project Name	Rev	
Custom	PT10SG	1.1	
Date: Tuesday, February 26, 2013		Sheet 57 of 104	

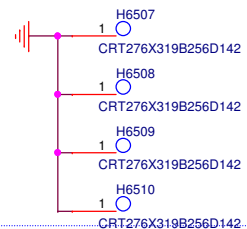
DC IN



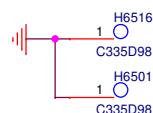
Battery Connector



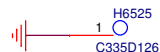
CPU : Screw Ex4
DXF : DETAIL A



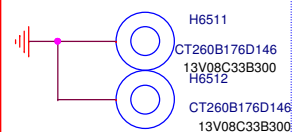
PCB : Screw Ax10
DXF : ITEAM A



Locate : Screw Dx1
DXF : ITEAM D



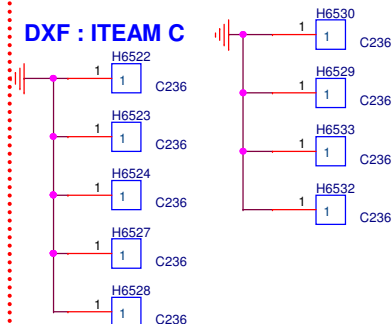
VGA : Screw Fx2
DXF : DETAIL B
TOP Side



1/23 R1.1

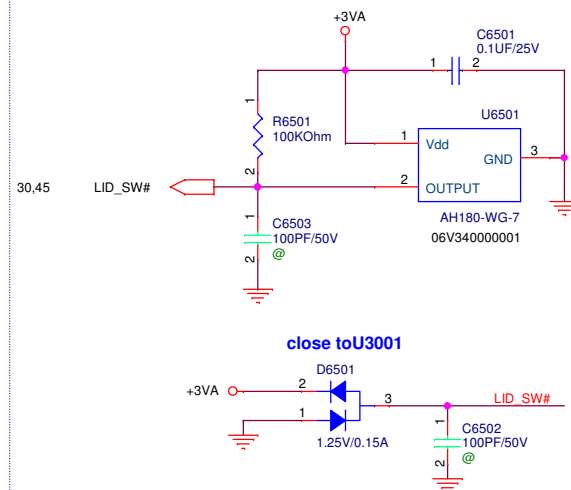
TOP/BOT : GND Cx5

DXF : ITEAM C

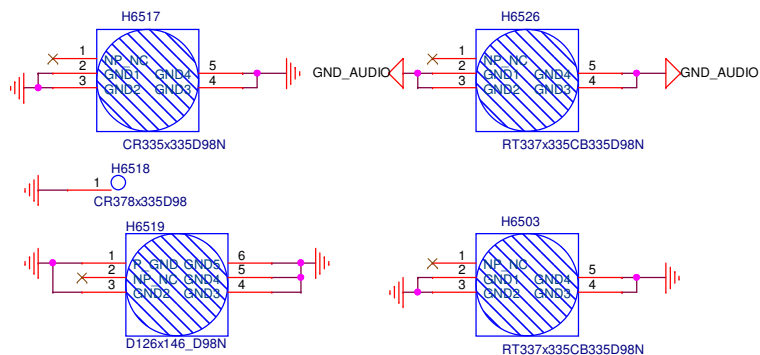


0921

LID Switch(Hall sensor)

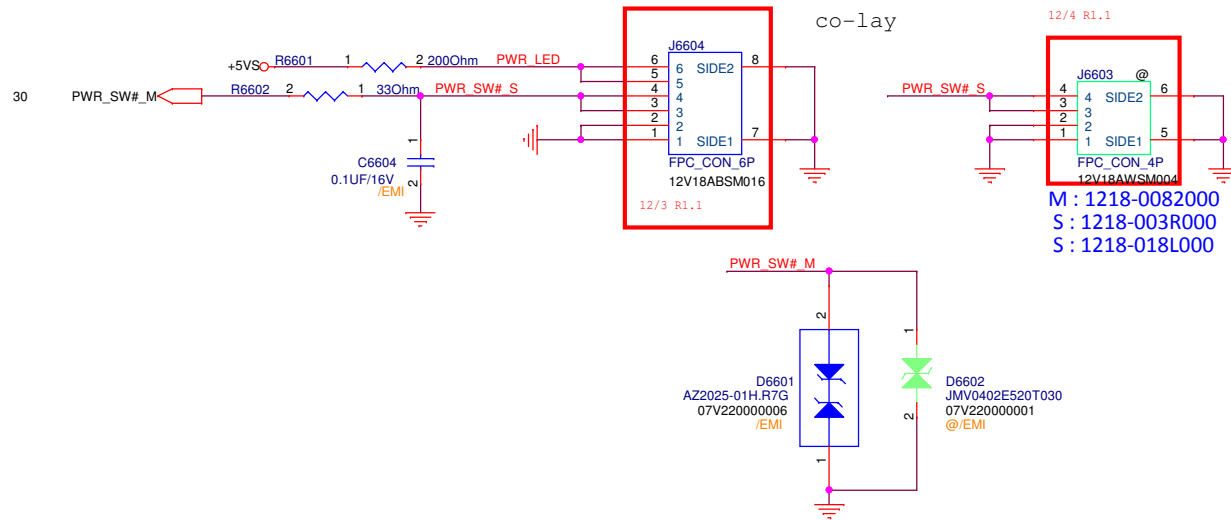


Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

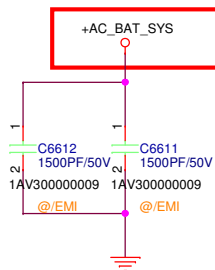


PEGATRON		Title ME_CONN,Skew Hole	
Size		Engineer: Tina Lee	
B		Project Name PT10SG	
Date: Tuesday, February 26, 2013		Sheet 65 of 104	
		Rev 1.1	

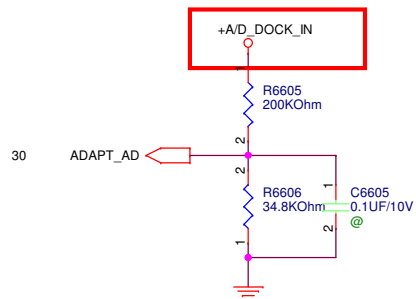
PWR BRD



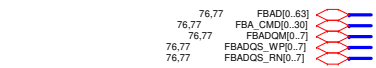
EMI



ADAPTOR VOLTAGE DETECTOR.



PEGATRON		Title : PEW BRD/IO BRD	
BG1-CSC-HW R&D Dept.5		Engineer: Tina Lee	
Size B	Project Name PT10SG		Rev 1.1
Date: Tuesday, February 26, 2013		Sheet 66 of 104	



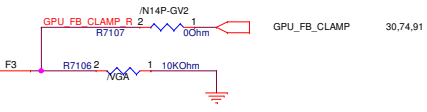
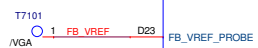
U7001B		2/14 FBA	
FBA00	E18	FBA_D0	
FBA01	F18	FBA_D1	
FBA02	E16	FBA_D2	
FBA03	F17	FBA_D3	
FBA04	D20	FBA_D4	
FBA05	D21	FBA_D5	
FBA06	F20	FBA_D6	
FBA07	E21	FBA_D7	
FBA08	E15	FBA_D8	
FBA09	D15	FBA_D9	
FBA10	F15	FBA_D10	
FBA11	F13	FBA_D11	
FBA12	C13	FBA_D12	
FBA13	B13	FBA_D13	
FBA14	E13	FBA_D13	
FBA15	D13	FBA_D14	
FBA16	B15	FBA_D15	
FBA17	C16	FBA_D16	
FBA18	A13	FBA_D17	
FBA19	A15	FBA_D18	
FBA20	B18	FBA_D19	
FBA21	A18	FBA_D20	
FBA22	A19	FBA_D21	
FBA23	C19	FBA_D22	
FBA24	B24	FBA_D23	
FBA25	C23	FBA_D24	
FBA26	A25	FBA_D25	
FBA27	A24	FBA_D26	
FBA28	A21	FBA_D27	
FBA29	B21	FBA_D28	
FBA30	C20	FBA_D29	
FBA31	C21	FBA_D30	
FBA32	B22	FBA_D31	
FBA33	B24	FBA_D32	
FBA34	Y22	FBA_D33	
FBA35	R23	FBA_D34	
FBA36	N26	FBA_D35	
FBA37	N26	FBA_D36	
FBA38	N23	FBA_D37	
FBA39	N24	FBA_D38	
FBA40	V23	FBA_D39	
FBA41	V22	FBA_D40	
FBA42	U23	FBA_D41	
FBA43	U22	FBA_D42	
FBA44	Y24	FBA_D43	
FBA45	AA24	FBA_D44	
FBA46	V22	FBA_D45	
FBA47	AA23	FBA_D46	
FBA48	AD27	FBA_D47	
FBA49	AB26	FBA_D48	
FBA50	AD26	FBA_D49	
FBA51	AC25	FBA_D50	
FBA52	AA27	FBA_D51	
FBA53	AA26	FBA_D52	
FBA54	W26	FBA_D53	
FBA55	Y25	FBA_D54	
FBA56	R26	FBA_D55	
FBA57	Y25	FBA_D56	
FBA58	N27	FBA_D57	
FBA59	R27	FBA_D58	
FBA60	V26	FBA_D59	
FBA61	V27	FBA_D60	
FBA62	W27	FBA_D61	
FBA63	W25	FBA_D62	
		FBA_D63	

FBA0M0	D19	FBA_D0M0
FBA0M1	D14	FBA_D0M1
FBA0M2	C17	FBA_D0M2
FBA0M3	C22	FBA_D0M3
FBA0M4	P24	FBA_D0M4
FBA0M5	W24	FBA_D0M5
FBA0M6	AA25	FBA_D0M6
FBA0M7	U25	FBA_D0M7

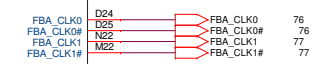
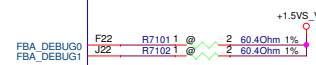
FBA0QS_WP0	E19	FBA_DQS_WP0
FBA0QS_WP1	C15	FBA_DQS_WP1
FBA0QS_WP2	B16	FBA_DQS_WP2
FBA0QS_WP3	B22	FBA_DQS_WP3
FBA0QS_WP4	R25	FBA_DQS_WP4
FBA0QS_WP5	W23	FBA_DQS_WP5
FBA0QS_WP6	AB26	FBA_DQS_WP6
FBA0QS_WP7	T26	FBA_DQS_WP7

FBA0QS_RN0	F19	FBA_DQS_RN0
FBA0QS_RN1	C14	FBA_DQS_RN1
FBA0QS_RN2	A16	FBA_DQS_RN2
FBA0QS_RN3	A22	FBA_DQS_RN3
FBA0QS_RN4	P25	FBA_DQS_RN4
FBA0QS_RN5	W22	FBA_DQS_RN5
FBA0QS_RN6	AB27	FBA_DQS_RN6
FBA0QS_RN7	T27	FBA_DQS_RN7

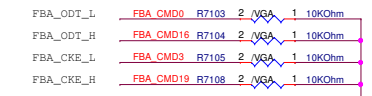
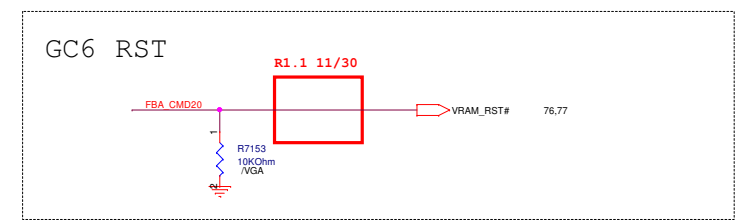
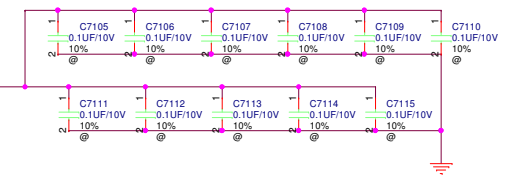
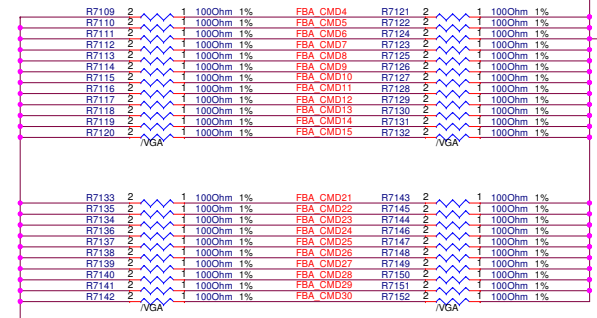
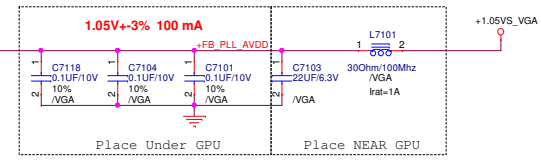
FB_PLLAVDD_1	F16
FB_PLLAVDD_2	P22
FB_PLLAVDD	
FB_LLAVDD	
GF117	GF117/GK208



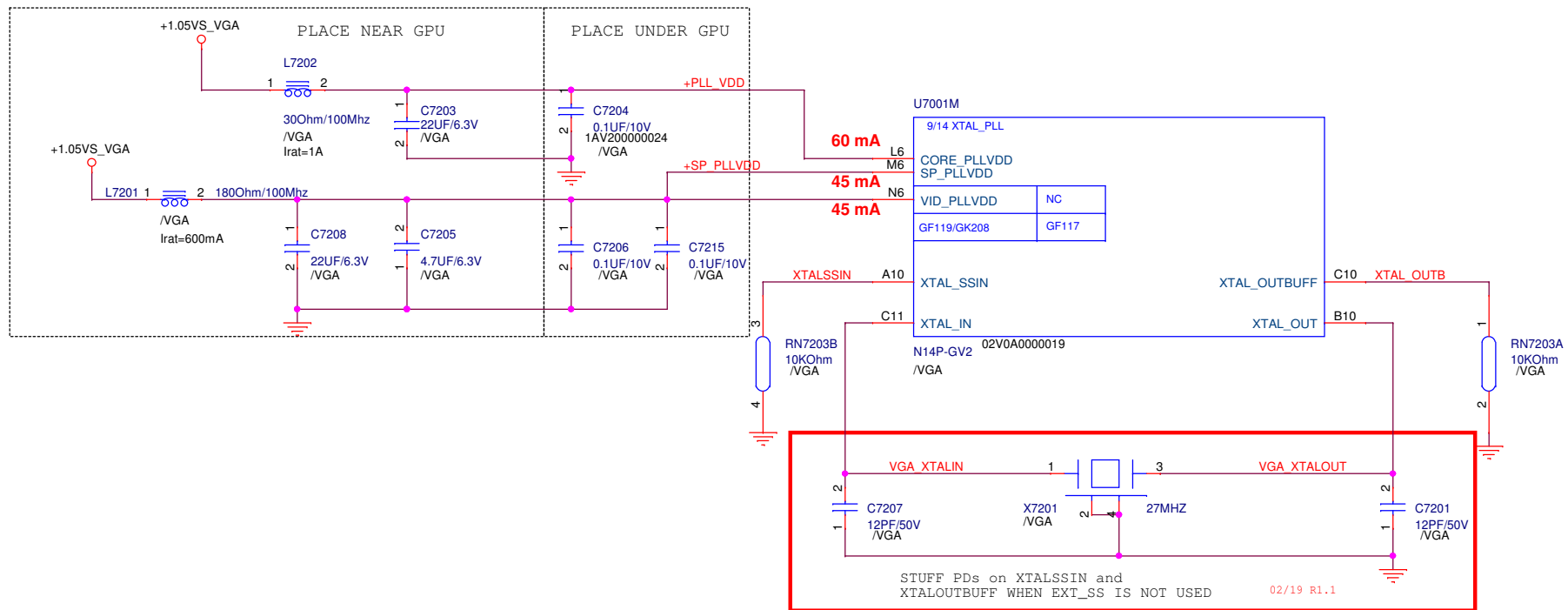
FBA_CMD0	C27	FBA_CMD0
FBA_CMD1	C26	FBA_CMD1
FBA_CMD2	E24	FBA_CMD2
FBA_CMD3	F24	FBA_CMD3
FBA_CMD4	D27	FBA_CMD4
FBA_CMD5	D26	FBA_CMD5
FBA_CMD6	P25	FBA_CMD6
FBA_CMD7	F26	FBA_CMD7
FBA_CMD8	F23	FBA_CMD8
FBA_CMD9	G22	FBA_CMD9
FBA_CMD10	G23	FBA_CMD10
FBA_CMD11	G24	FBA_CMD11
FBA_CMD12	F27	FBA_CMD12
FBA_CMD13	G25	FBA_CMD13
FBA_CMD14	G27	FBA_CMD14
FBA_CMD15	G26	FBA_CMD15
FBA_CMD16	M24	FBA_CMD16
FBA_CMD17	M23	FBA_CMD17
FBA_CMD18	K24	FBA_CMD18
FBA_CMD19	M27	FBA_CMD19
FBA_CMD20	M26	FBA_CMD20
FBA_CMD21	M25	FBA_CMD21
FBA_CMD22	K26	FBA_CMD22
FBA_CMD23	K22	FBA_CMD23
FBA_CMD24	J23	FBA_CMD24
FBA_CMD25	J25	FBA_CMD25
FBA_CMD26	J24	FBA_CMD26
FBA_CMD27	K27	FBA_CMD27
FBA_CMD28	K25	FBA_CMD28
FBA_CMD29	J27	FBA_CMD29
FBA_CMD30	J26	FBA_CMD30
FBA_CMD31		



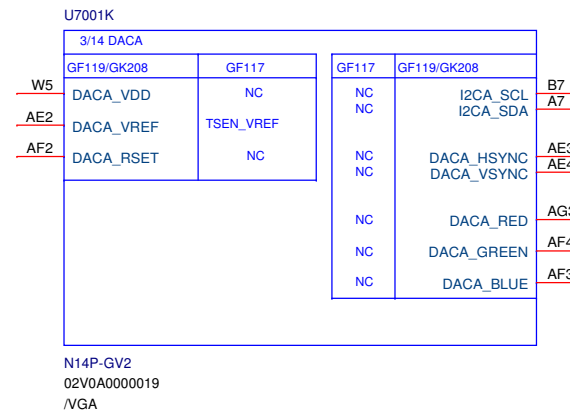
FBA_WCK01	D18
FBA_WCK01#	C18
FBA_WCK23	D17
FBA_WCK23#	T24
FBA_WCK45	U24
FBA_WCK45#	V24
FBA_WCK67	V25
FBA_WCK67#	



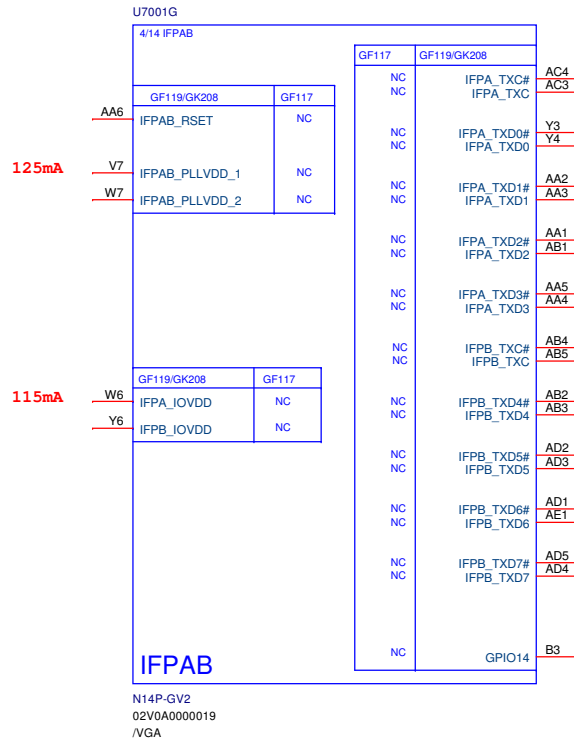
<http://forum.hocvienit.vn>



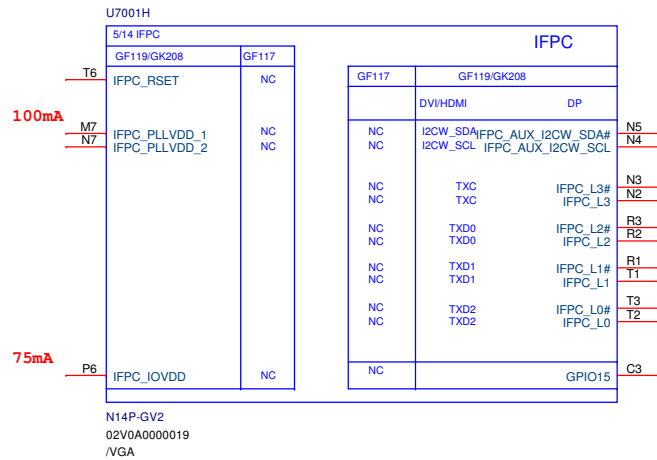
UNconnected
Leave DACA_VDD floating
DACA_VREF, DACA_RSET, IO floating



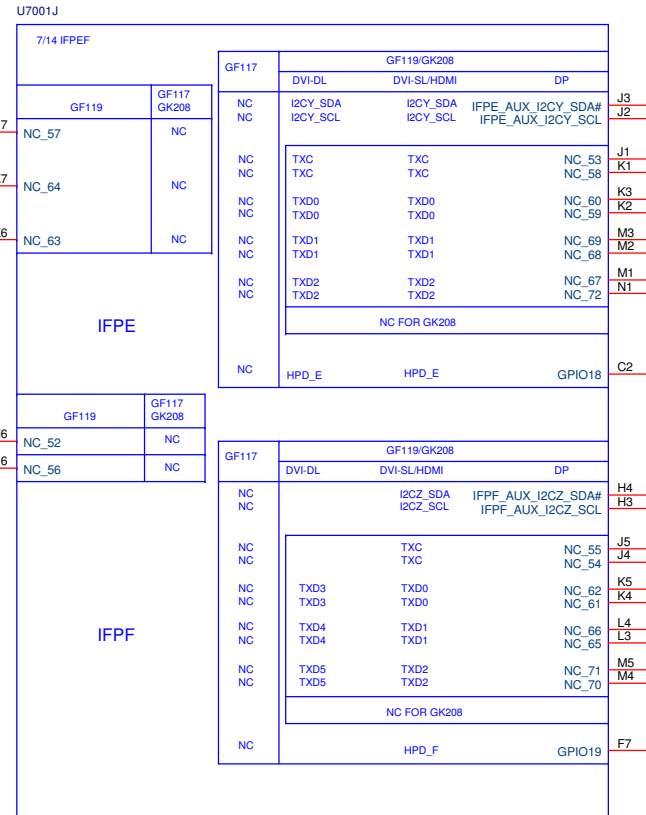
LVDS



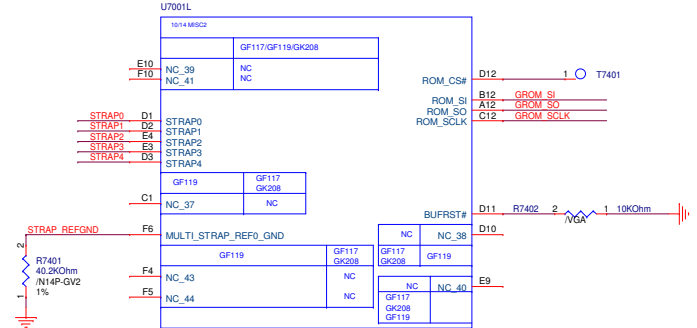
HDMI



Check it



<http://forum.hocvienit.vn>



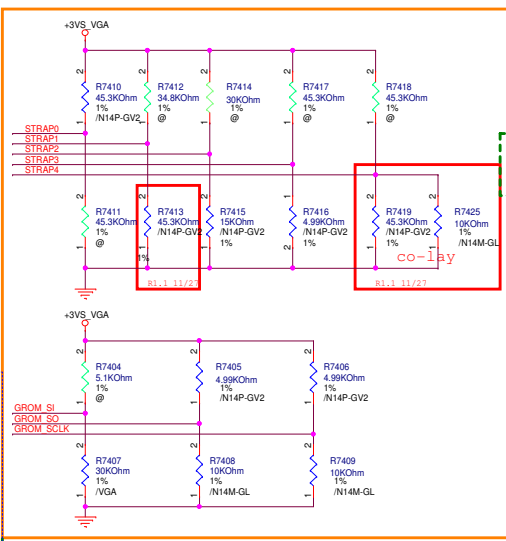
BINARY STRAP MODE MAPPING for N14M-GL

Pin Name	Mapping
ROM_SCLK	SMB_ALT_ADDR Pull down 10K
ROM_SI	SMB_VENDOR Pull down 10K
ROM_SO	VGA_DEVICE Pull down 10K
STRAP0	RAM_CFG[0]
STRAP1	RAM_CFG[1]
STRAP2	RAM_CFG[2]
STRAP3	RAM_CFG[3]
STRAP4	PCI_MAX_SPEED Pull down 10K

RAM_CFG[3:0]

Vendor	Part Number	Strap
Micron	MT41J128M16JT-093G:K (NA)	0x1 (0001)
Micron	MT41J128M16JT-107G:K (NA)	0x1 (0001)
Hynix	H5TQ4G63MFR-11C (TBD)	0x3 (0011)
Hynix	H5TQ4G63AFR-11C (0315-01110TB)	0x4 (0100)
Samsung	K4W2G1646E-BC1A (0315-010B0TB)	0x5 (0101)
Samsung	K4W2G1646E-BC11 (0315-00XJ0TB)	0x5 (0101)
Hynix	H5TQ2G63DFR-N0C (0315-010C0TB)	0x6 (0110)
Hynix	H5TQ2G63DFR-11C (0315-00UD0TB)	0x6 (0110)
Samsung	K4W4G1646E-BC11 (0315-00WN0TB)	0x6 (0111)
Micron	MT41K256M16HA-107G:E (0315-00X90TB)	0xD (1101)

1: Pull up 10k
0: Pull down 10k



STRAP0(1,1,1,1 pu 45K)

```

USER[3:0]
0 2 1 0 PANEL VS/HS
0 0 0 0 XGA
0 0 0 1 XGA
0 0 1 0 SXGA
0 0 1 1 SXGA+
1 1 1 1 RNDV N/A
  
```

STRAP1(0,1,1,1 PD 45K)

```

3GIO_PADCFG[3:0] 11/13
0 2 1 0 gen3 support
others RESERVED
  
```

ROM_SO (1,0,0,0 PU 5K)

```

LOGICAL BIT
3 FB[1]
2 FB[0]
1 SMB_ALT_ADDR
0 VGA_DEVICE
  
```

4.99K PU 1000 PD 0000
10.0K PU 1001 PD 0001
15.0K PU 1010 PD 0010
20.0K PU 1011 PD 0011
24.9K PU 1100 PD 0100
30.1K PU 1101 PD 0101
34.8K PU 1110 PD 0110
45.3K PU 1111 PD 0111

STRAP2 (0,0,1,0 PD 15K)

```

LOGICAL BIT
0 PCI_DEVID[0]
1 PCI_DEVID[1]
2 PCI_DEVID[2]
3 PCI_DEVID[3]
  
```

ROM_SCLK for GV2 QS

```

LOGICAL BIT
3 PCI_DEVID[4]
2 SUB_VENDOR
1 PCI_DEVID[5]
0 PEX_PLL_EN_TERM
  
```

STRAP3 (0,0,0,0 PD 5K)

```

LOGICAL BIT
0 SOR0_EXPOSED
1 SOR1_EXPOSED
2 SOR2_EXPOSED
3 SOR3_EXPOSED
  
```

STRAP4 (0,1,1,1 PD 45K)

```

LOGICAL BIT
0 SOR0_EXPOSED
1 SOR1_EXPOSED
2 SOR2_EXPOSED
3 SOR3_EXPOSED
  
```

PCI_DEVID[3..0]
N12P-GV2 ES --> 0x12AD ~ 1 1 0 1 --> pull up 30K
N12P-GV2 QS --> 0x1292 ~ 0 0 1 0 --> pull down 15K

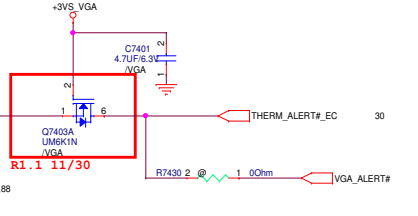
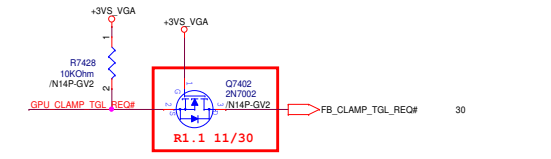
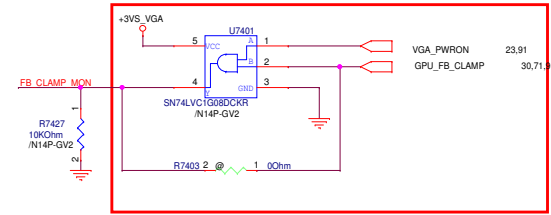
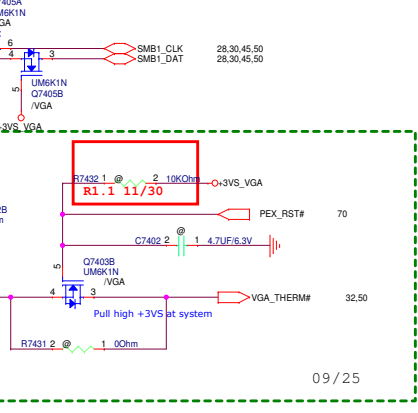
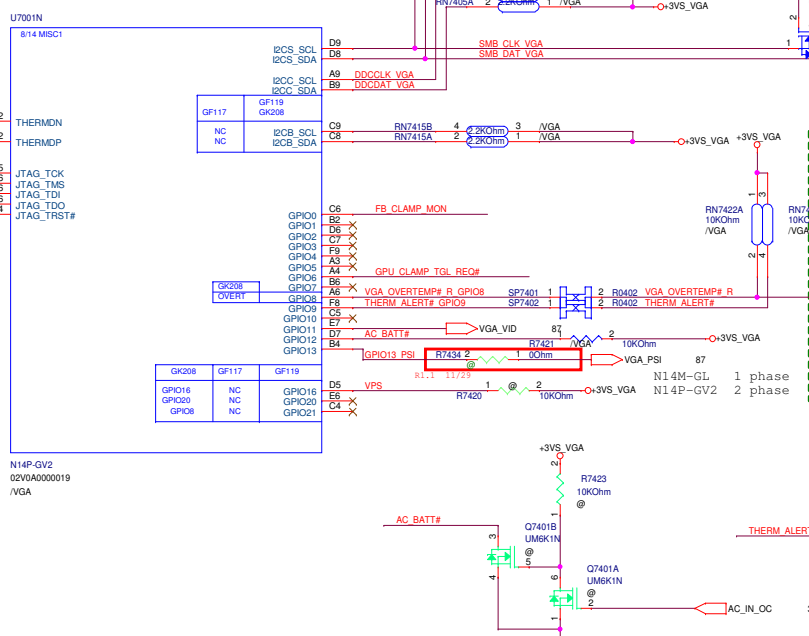
ROM_SI RAMCONFIG (0,1,0,1 PD 30K) 11/30 base on Nv RVL v12

Micron 128Mx16

Vendor	RVL	AVL	Strap
Micron	**MT41J128M16JT-093G:K (NA)	0x5 (0101)	Pull down 30k
Micron	MT41J128M16JT-107G:K (NA)	0x5 (0101)	Pull down 30k
Micron	(TBD)	0x5 (0101)	Pull down 30k
Samsung	** K4W2G1646E-BC1A (0315-010B0TB)	0x7 (0111)	Pull down 45k
Samsung	K4W2G1646E-BC11 (0315-00XJ0TB)	0x7 (0111)	Pull down 45k

**** RVL list part**

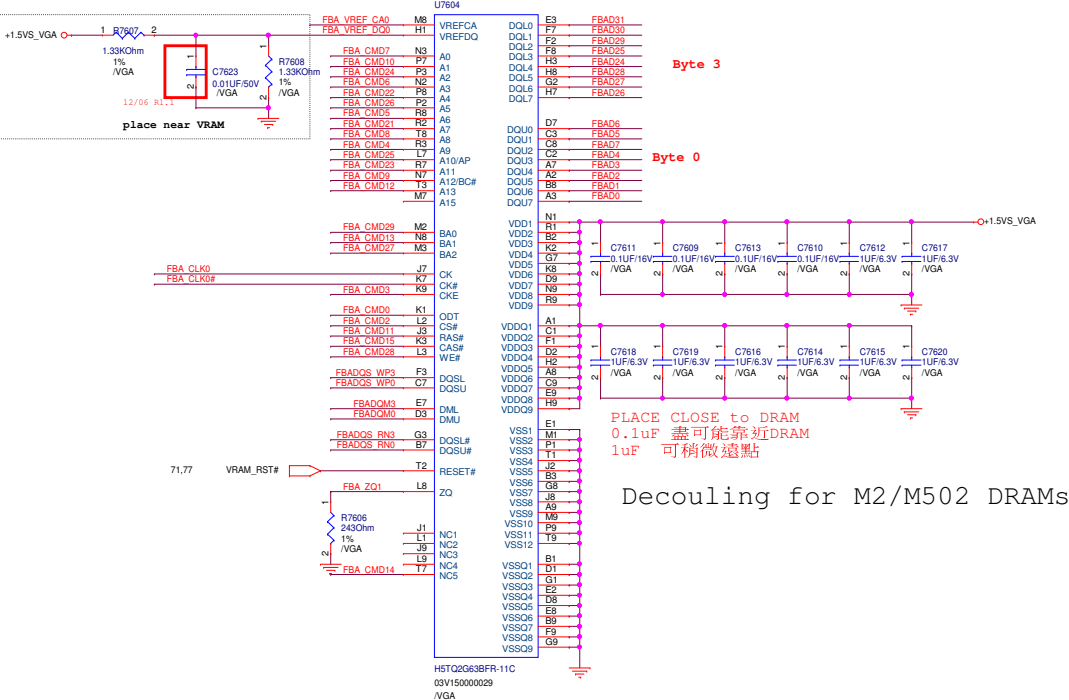
MULTI-LEVEL MODE STRAPPING for N14P-GV2/GS



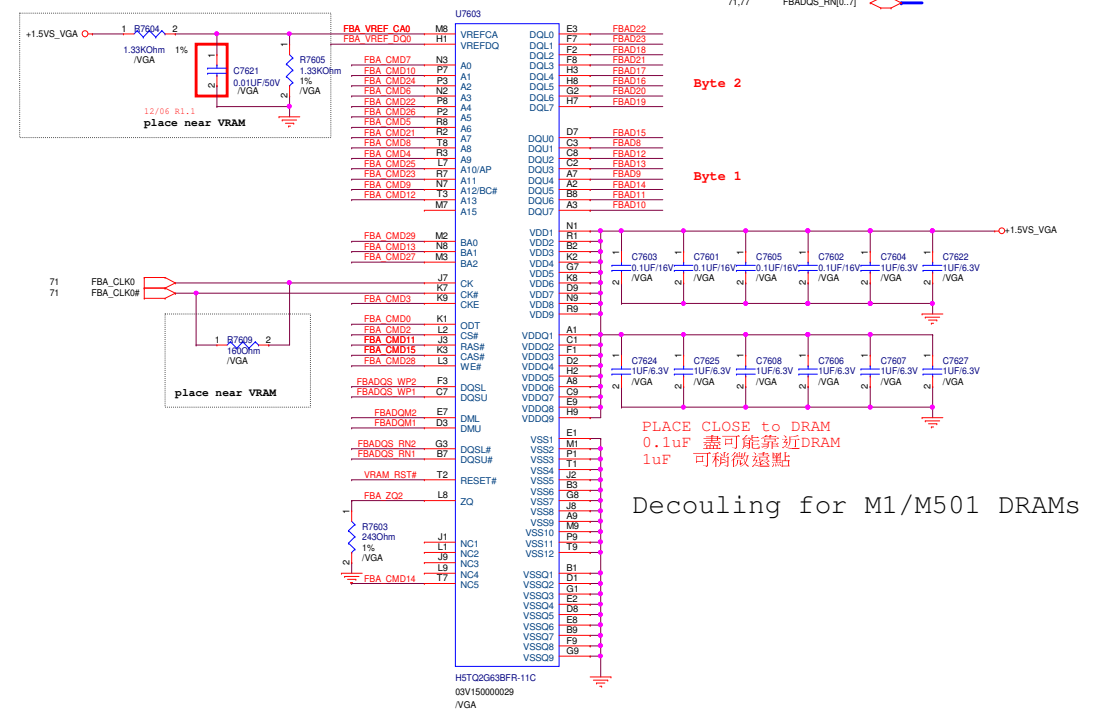
<http://forum.hocvienit.vn>

FBA Patyition 31..0 RANK 0

TOP SIDE --- M2

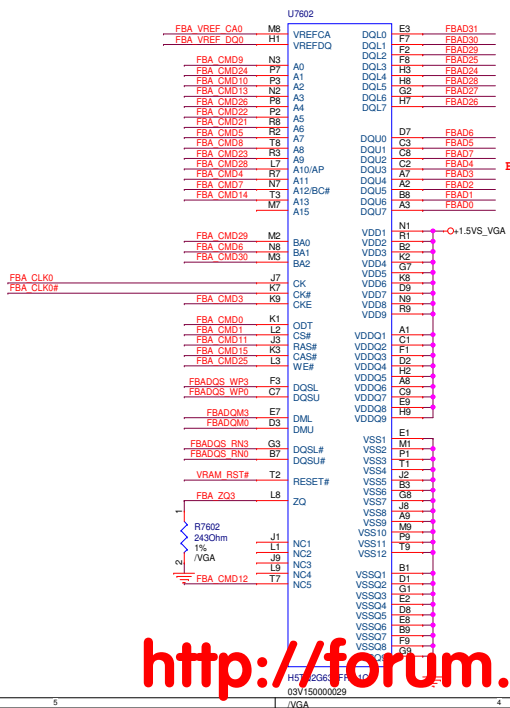


TOP SIDE --- M1

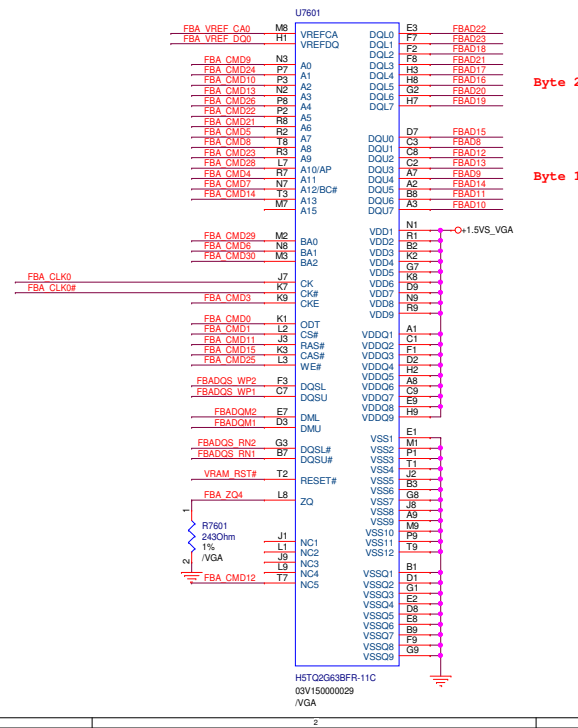


FBA Patyition 31..0 RANK 1

BOT SIDE --- M502



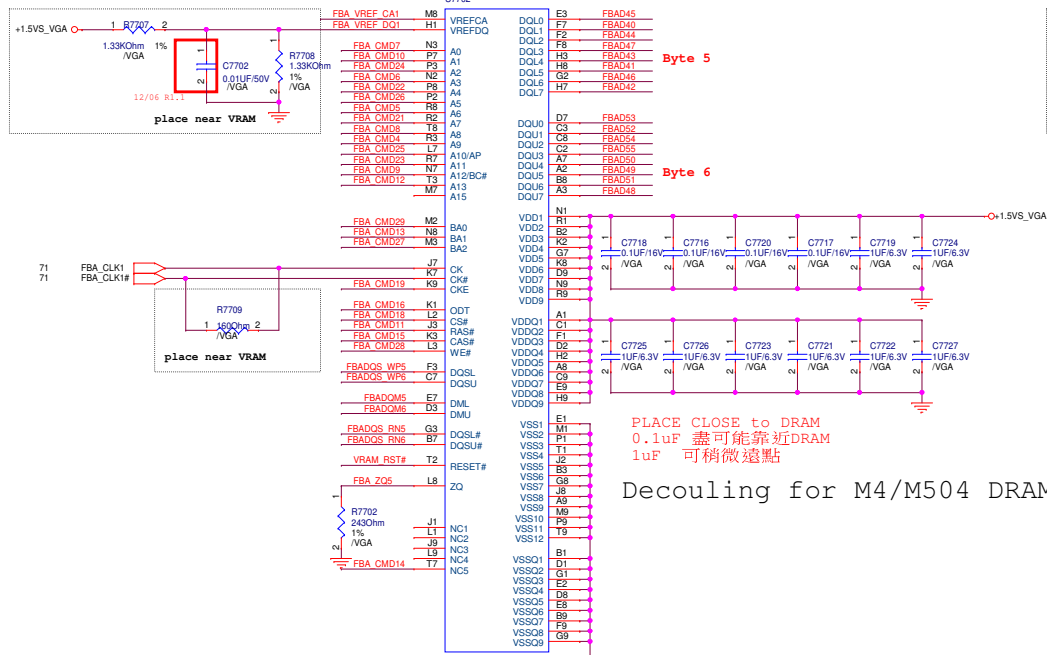
BOT SIDE --- M501



<http://forum.hocvienit.vn>

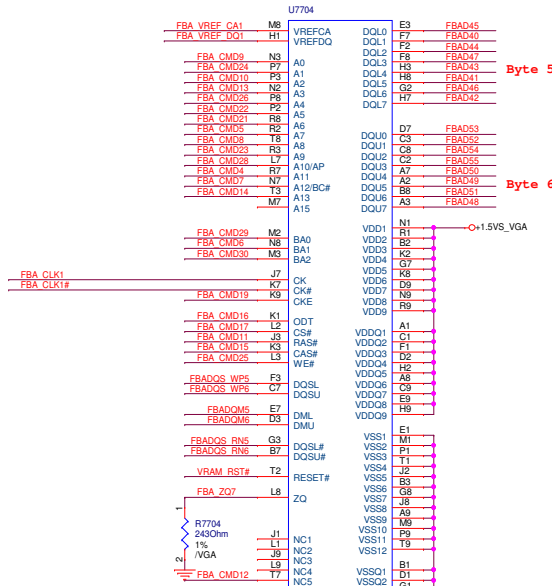
FBA Patyition 63..32 RANK 0

TOP SIDE --- M4

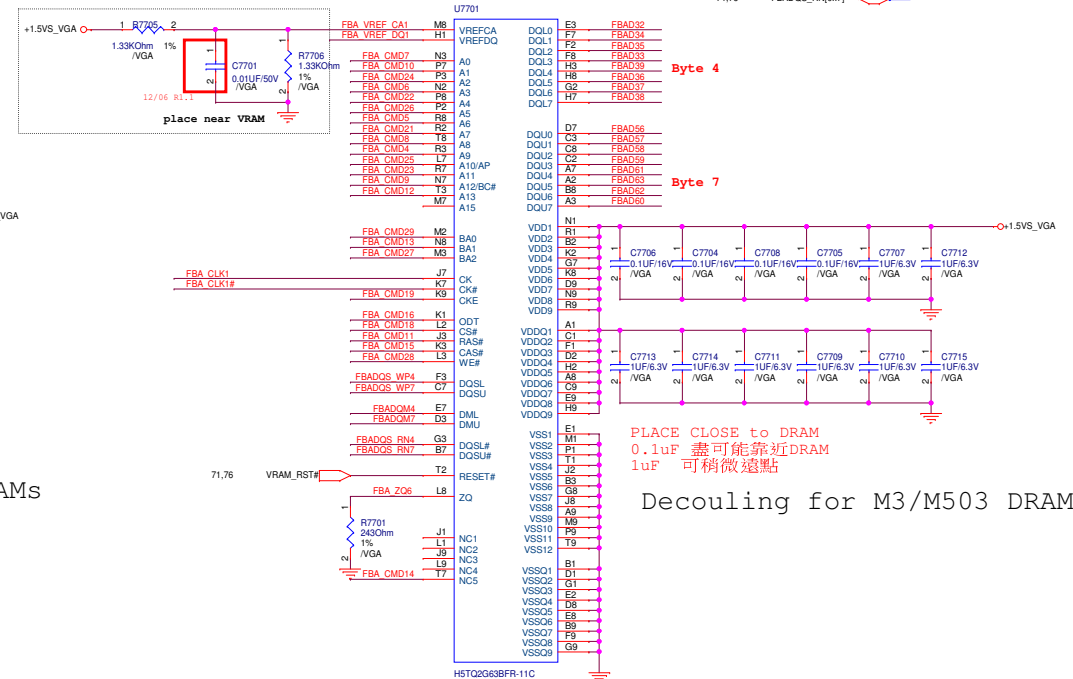


FBA Patyition 63..32 RANK 1

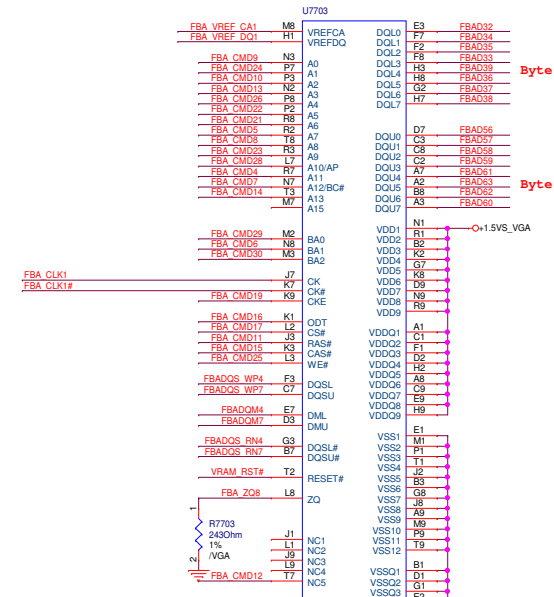
BOT SIDE --- M504



TOP SIDE --- M3

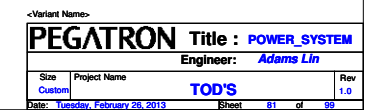


BOT SIDE --- M503

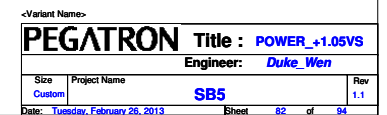


<http://forum.hocvienit.vn>

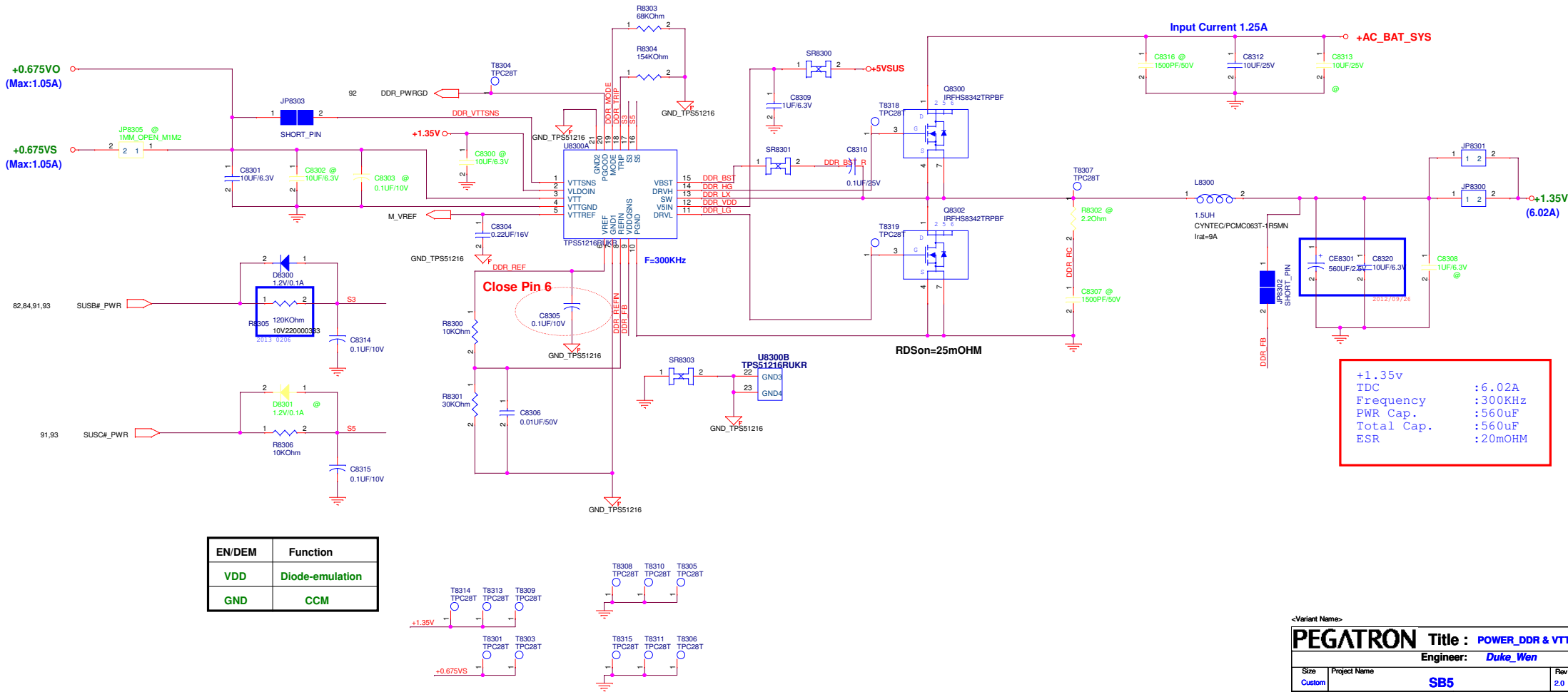
<http://forum.hocvienit.vn>



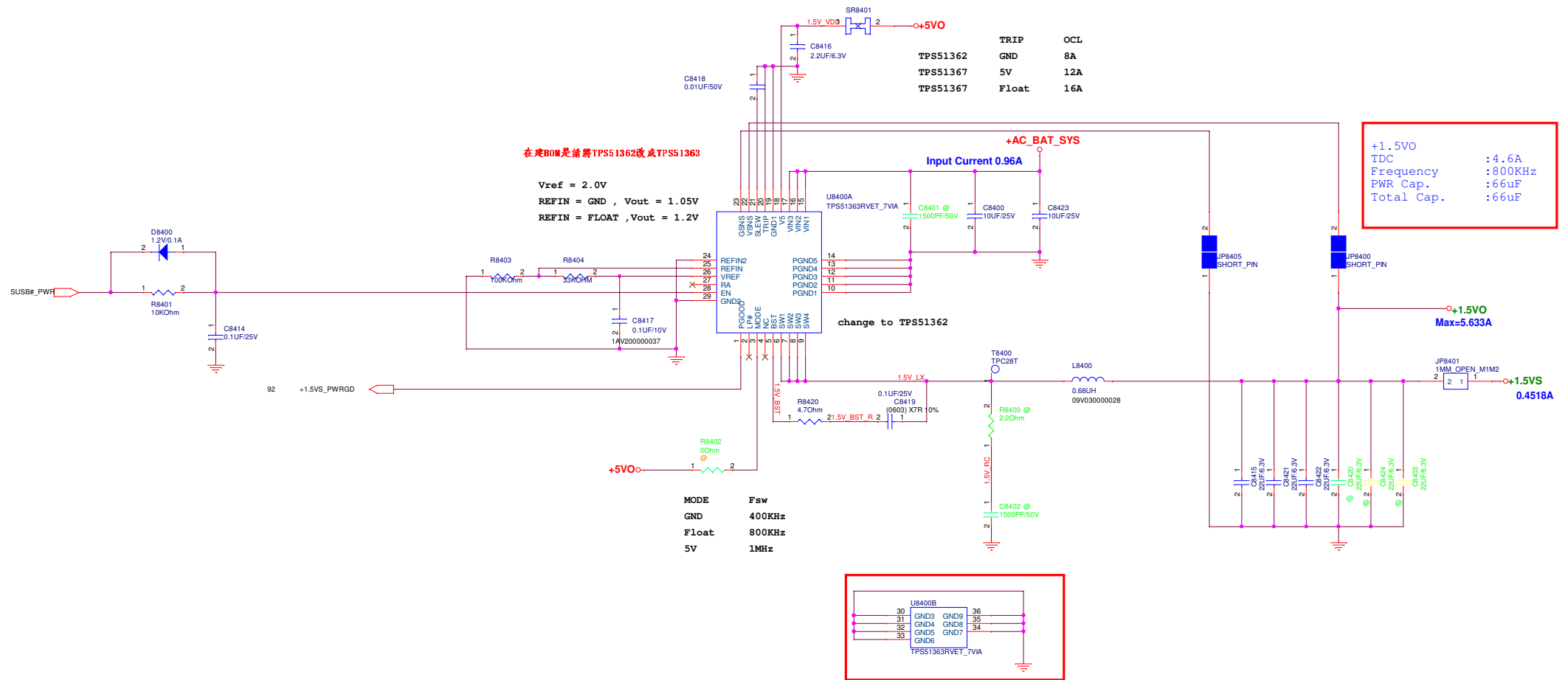
<http://forum.hocvienit.vn>



DDR & VTT POWER SUPPLY

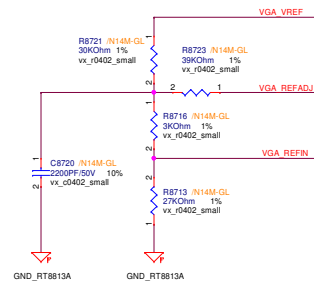


1.5VS POWER SUPPLY

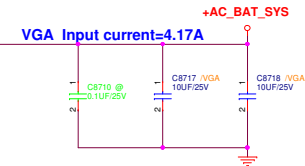
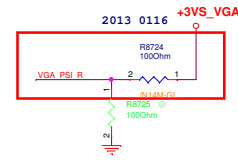


5					4					3					2					1										
D																														
C																														
B																														
A																														
<div><Variant Name> PEGATRON Title :POWER_N/A Engineer: <table border="1"><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>Custom</td><td></td><td>1.1</td></tr></table> Date: Tuesday, February 26, 2013 Sheet 86 of 94</div>																									Size	Project Name	Rev	Custom		1.1
Size	Project Name	Rev																												
Custom		1.1																												
5					4					3					2					1										

VGA_CORE POWER SUPPLY



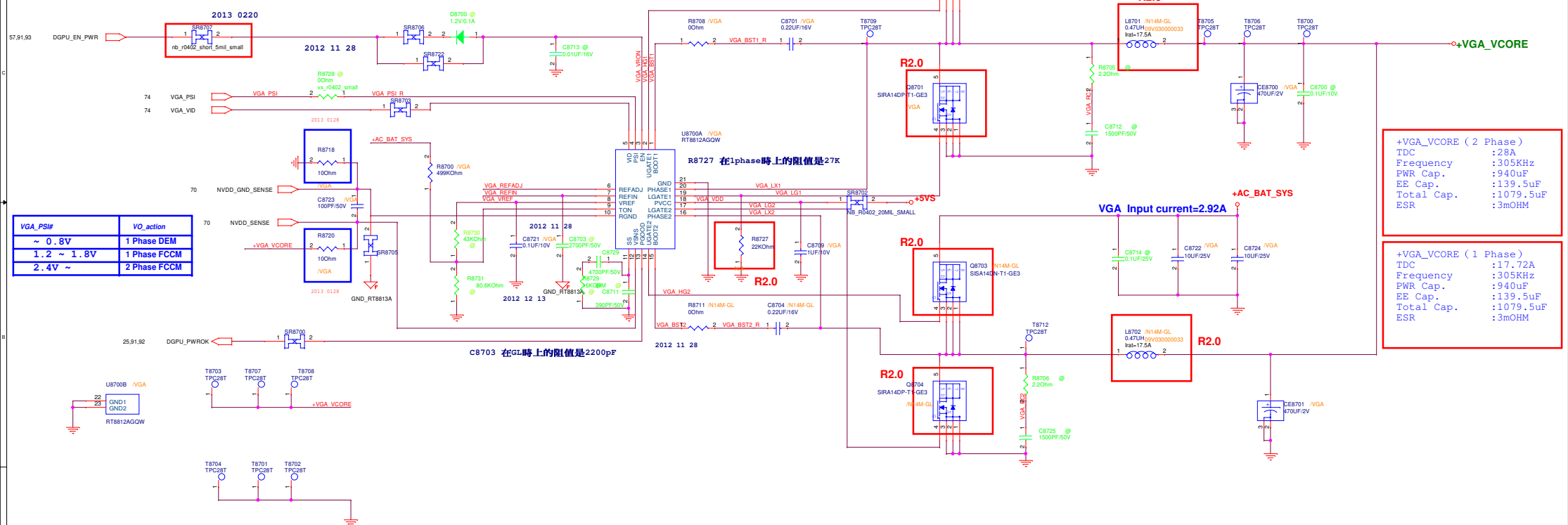
	N14M-GL	N14P-GV2
R8723	39K	20K
R8721	30K	20K
R8716	3K	2K
R8713	27K	18K
C8720	2.2nF	2.7nF
R8727	22K	20K
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.9V	0.9V
L8701	0.47uH	0.36uH
L8702	0.47uH	0.36uH
Q8701	S1RA14	S1RA10
Q8704	S1RA14	S1RA10
optional naming	/N14M-GL	/N14P-GV2



1 PHASE
N14M-GL
EDP=24.33A
TDC=17.72A
OCP: 40A

2 PHASE
N14P-GV2
EDP=33A
TDC=28A
OCP: 70A

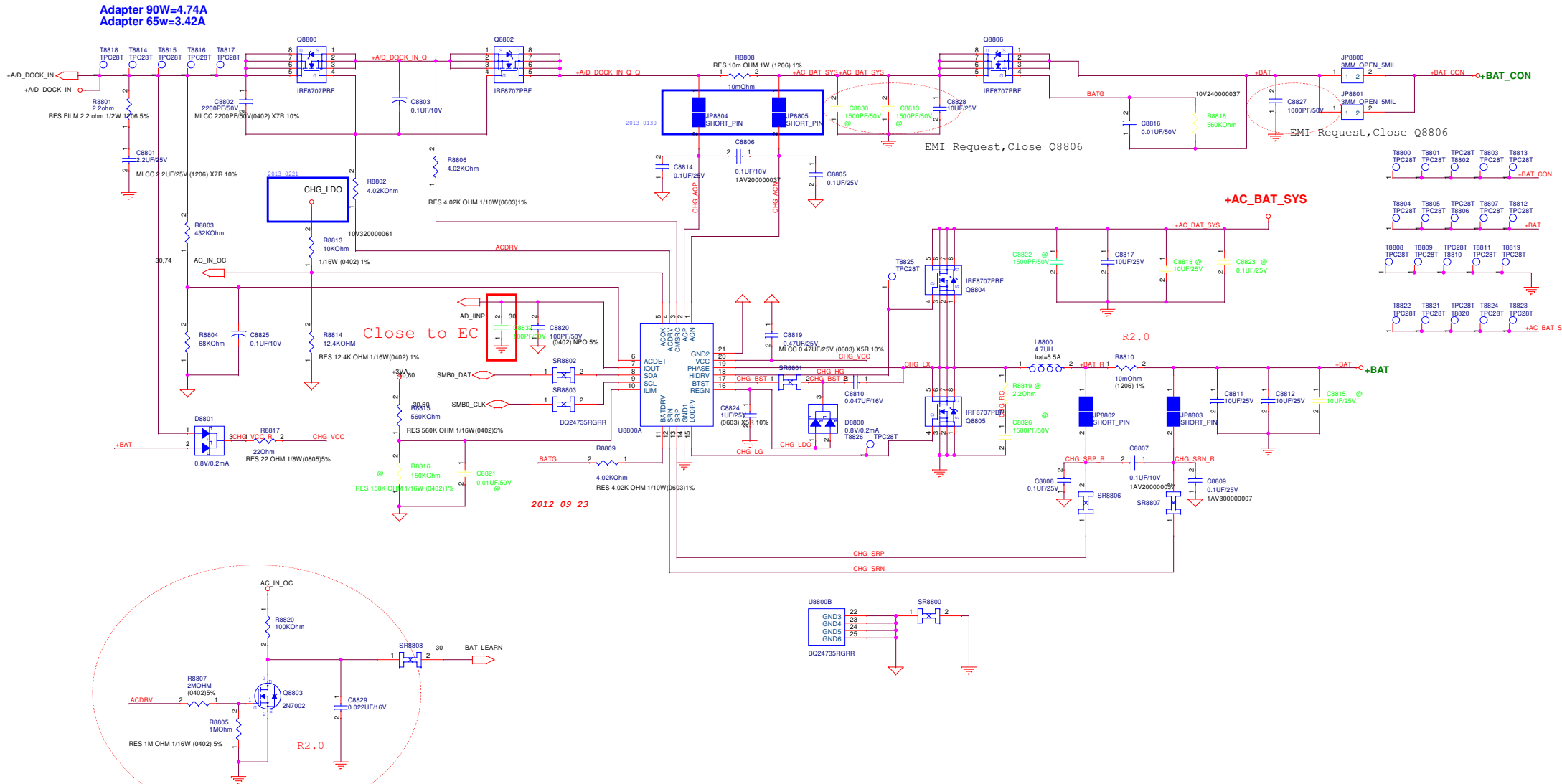
2 PHASE
N14P-GS
EDP=36A
TDC=28A
OCP: 70A



```
+VGA_VCORE ( 2 Phase )
TDC           :28A
Frequency      :305KHz
PWR Cap.      :940uF
EE Cap.       :139.5uF
Total Cap.    :1079.5uF
ESR           :3mOHM
```

```
+VGA_VCORE (1 Phase)
TDC           :17.72A
Frequency      :305KHz
PWR Cap.      :940uF
EE Cap.       :139.5uF
Total Cap.     :1079.5uF
ESR            :3mOHM
```

BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: **Duke Wen**

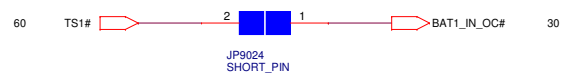
Size	Project Name	Rev
------	--------------	-----

Custom	SB5	2.0
--------	-----	-----

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5	4	3	2	1												
D				D												
C				C												
B				B												
A				A												
<div><Variant Name></div> <table border="1"><tr><td colspan="3">PEGATRON Title :POWER_N/A</td></tr><tr><td colspan="3">Engineer:</td></tr><tr><td>Size A</td><td>Project Name</td><td>Rev 1.1</td></tr><tr><td colspan="2">Date: Tuesday, February 26, 2013</td><td>Sheet 89 of 99</td></tr></table>					PEGATRON Title :POWER_N/A			Engineer:			Size A	Project Name	Rev 1.1	Date: Tuesday, February 26, 2013		Sheet 89 of 99
PEGATRON Title :POWER_N/A																
Engineer:																
Size A	Project Name	Rev 1.1														
Date: Tuesday, February 26, 2013		Sheet 89 of 99														

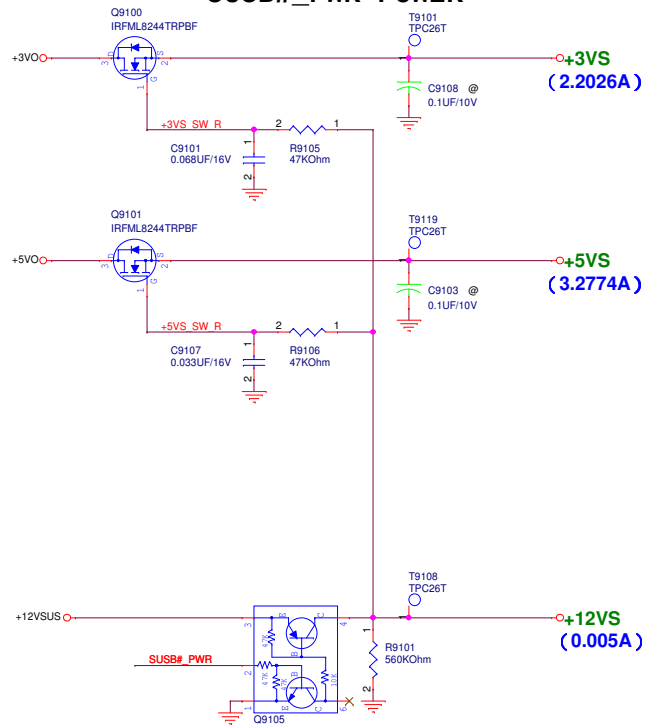
BATTERY IN DETECT

<Variant Name>

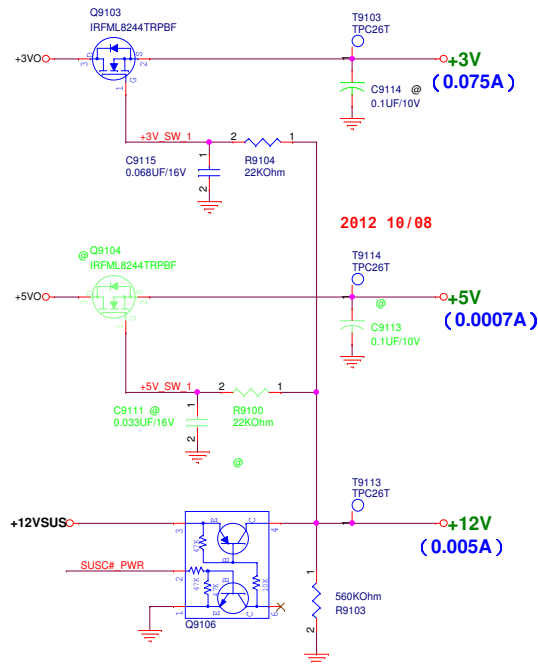
PEGATRON Title : **POWER_DETECT**Engineer: **Duke_Wen**

Size	Project Name	Rev
Custom	SB5	1.1
Date: Tuesday, February 26, 2013	Sheet 90 of 99	

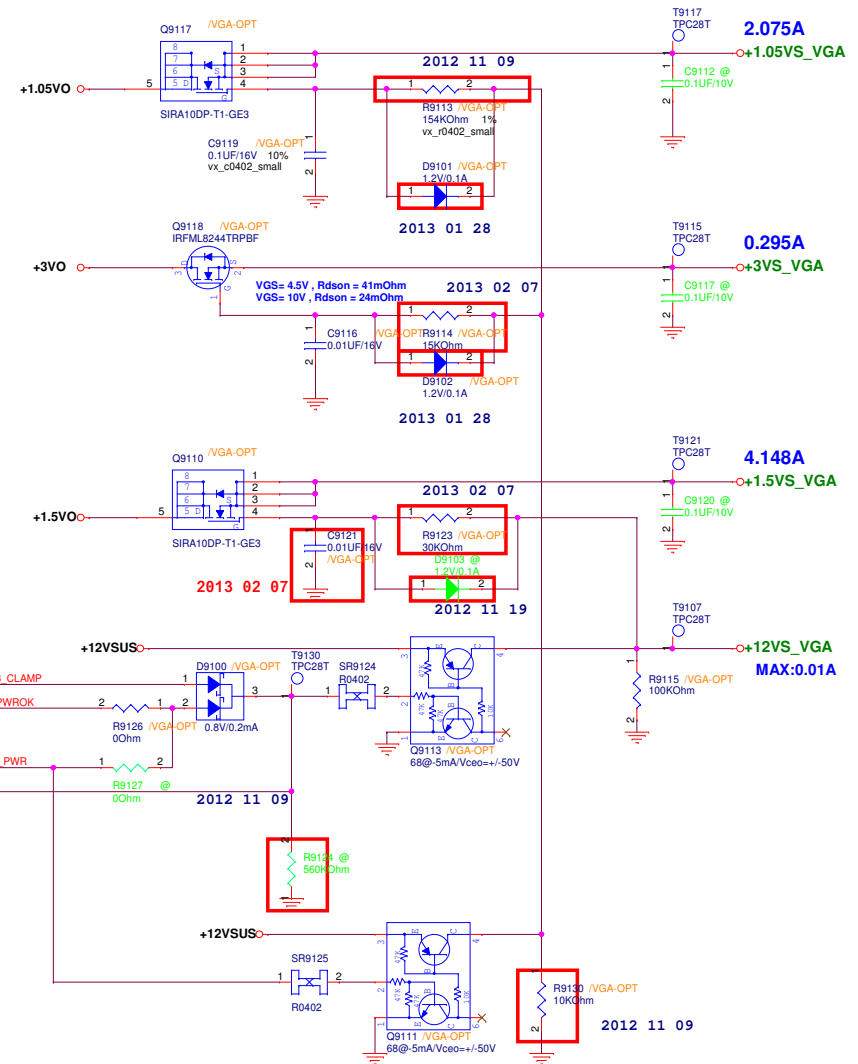
SUSB#_PWR POWER



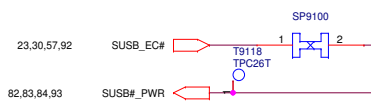
SUSC#_PWR POWER 2012 09 21



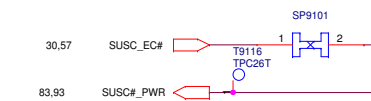
DSC#_PWR POWER(DGPU)



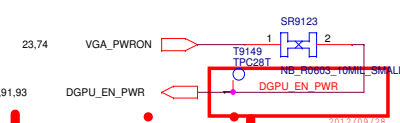
SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



DSC_VGA_PWR POWER Control



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<Variant Name>

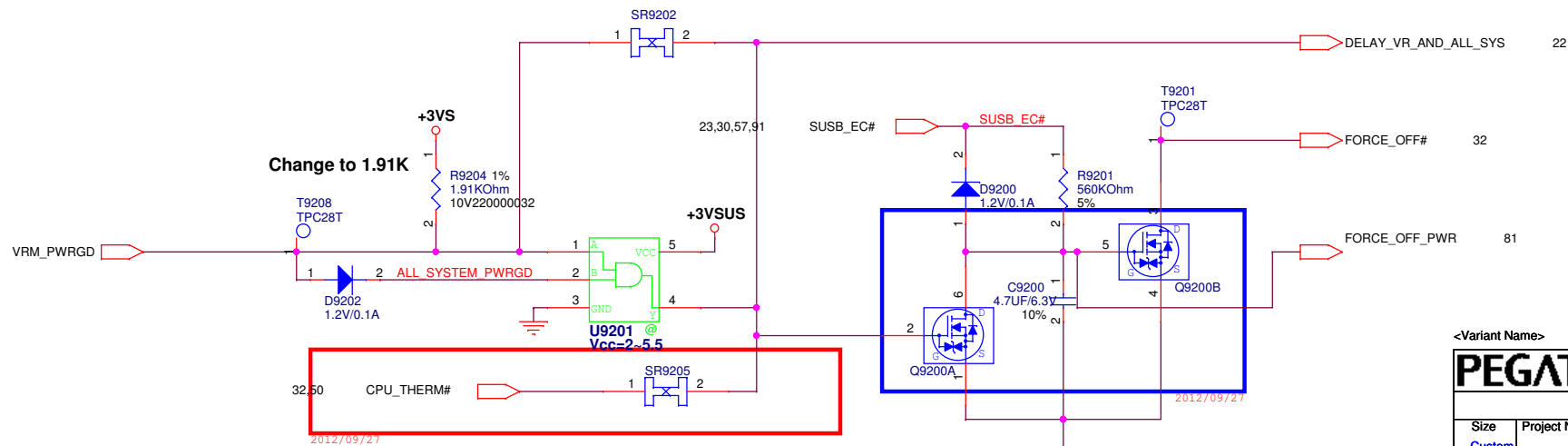
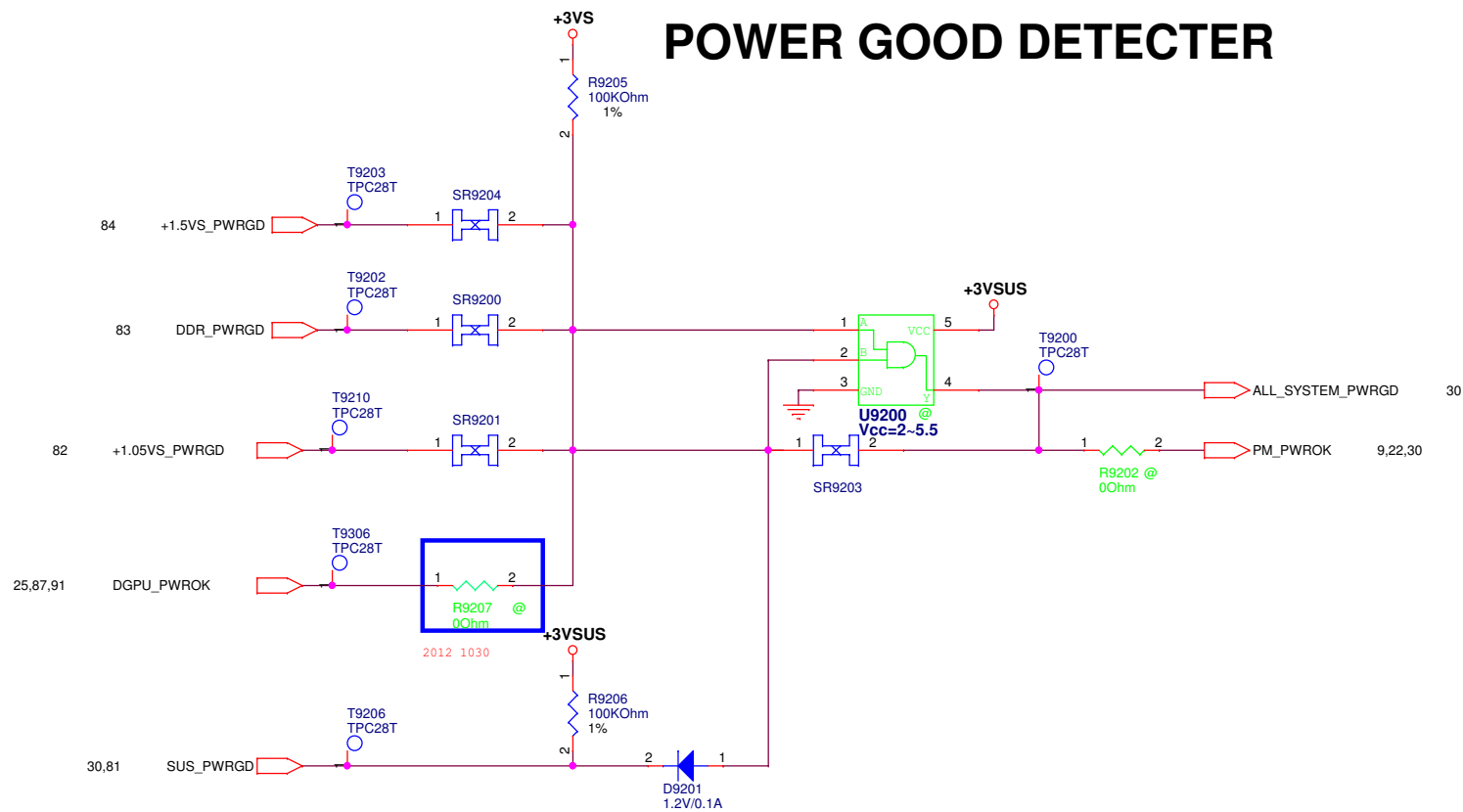
PEGATRON Title : POWER_LOAD SWITCH

Engineer: Mario_tsal

Size | Project Name | CP1 | Rev 1.0

Date: Tuesday, February 26, 2013 | Sheet 91 of 94

POWER GOOD DETECTOR



<Variant Name>

PEGATRON Title : **POWER_PROTECT**

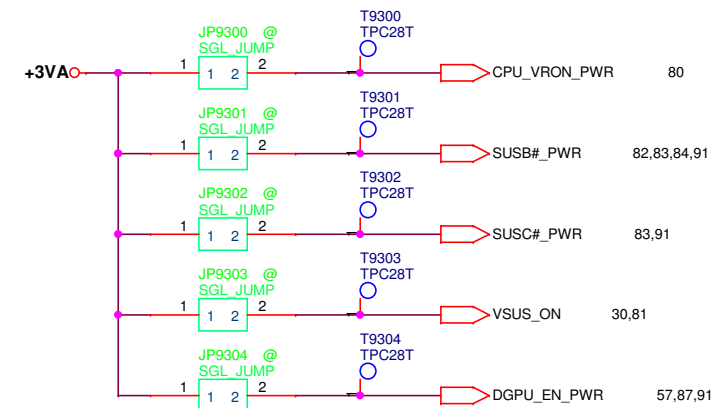
Engineer: **Duke_Wen**

Size	Project Name	Rev
Custom	SB5	2.0

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FOR POWER TEST

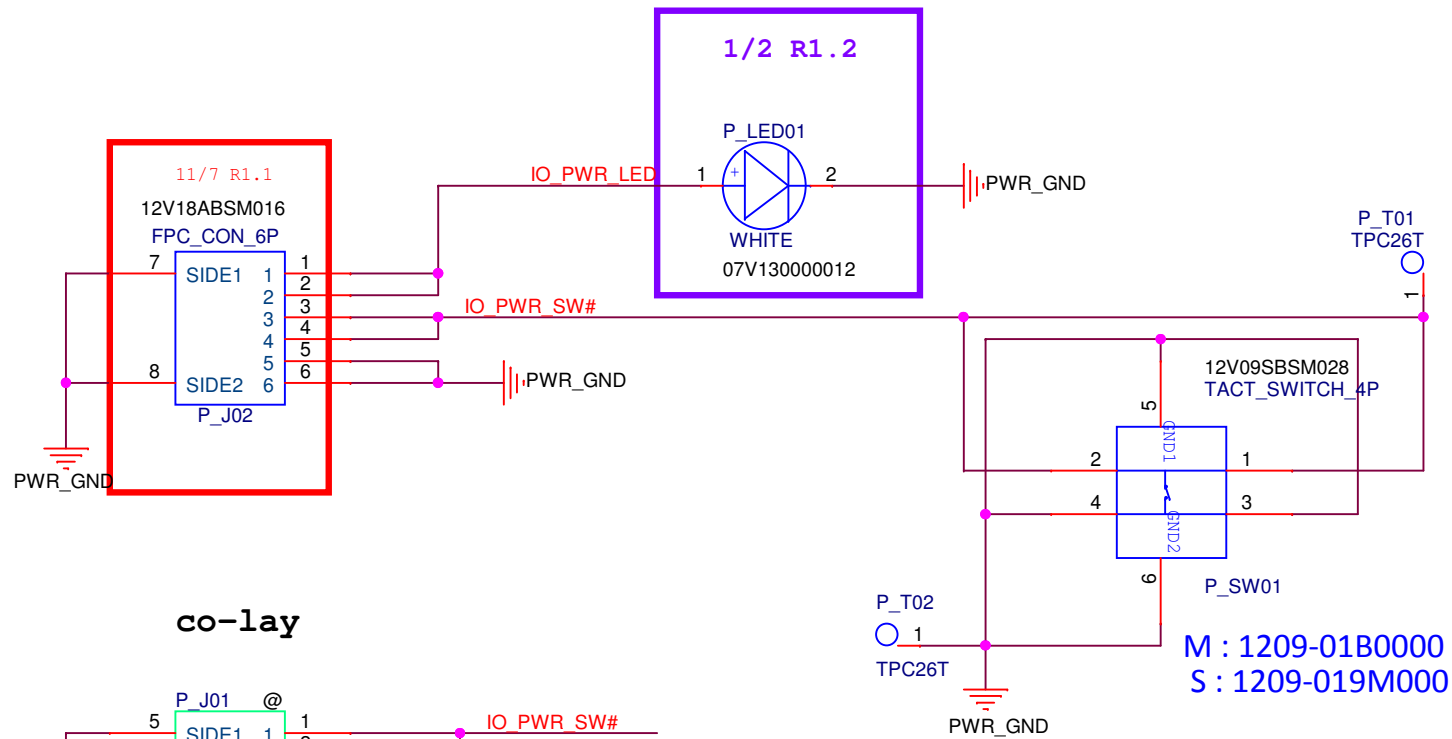


<Variant Name>

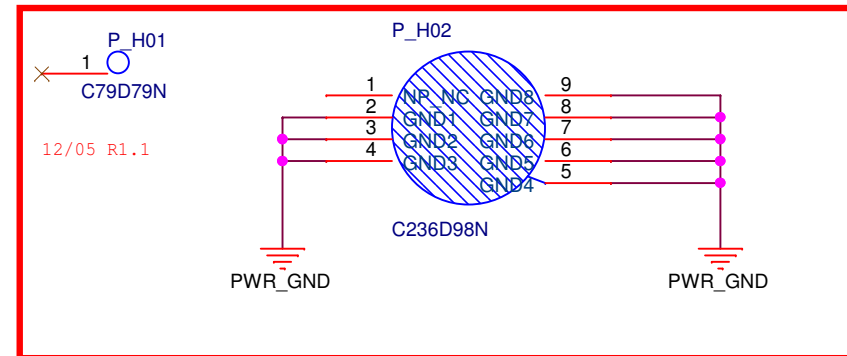
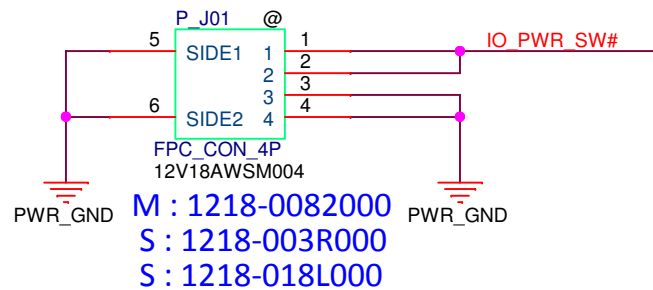
PEGATRON		Title : POWER_SIGNAL	
		Engineer: Duke_Wen	
Size	Project Name	SB5	Rev 2.0
Custom			
Date: Tuesday, February 26, 2013		Sheet 93 of 94	

PEGATRON		Title : Power History
		Keywords: Juke , Blues
File	Description	File
Power	Juke	Blues

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co-lay



PEGATRON			Title : PWR BD	
BG1-HW R&D Dept.3			Engineer:	
Size A	Project Name PT10SG			Rev 1.1
Date: Tuesday, February 26, 2013			Sheet	100 of 102

TP_GND

TP_+5VS

TP_B

TP_J01

SIDE2

SIDE1

IO_TP_CLK

IO_TP_DAT

IO_TP_LEFT

IO_TP_RIGHT

FPC_CON_6P

12V18ABSM016

TP-U01

TP_+5VS

1

2 IO TP CLK

3 IO TP DAT

4

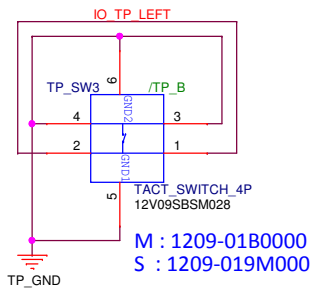
5 IO TP SMB CLK

6 IO TP SMB DAT

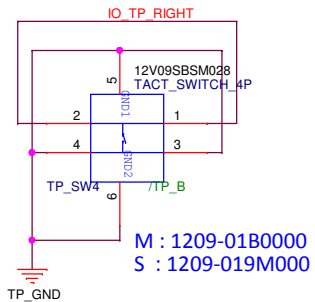
SMDPAD_6P

TP_GND

TP_MODEL	BOM Optional
TM-01146-003	TP_B

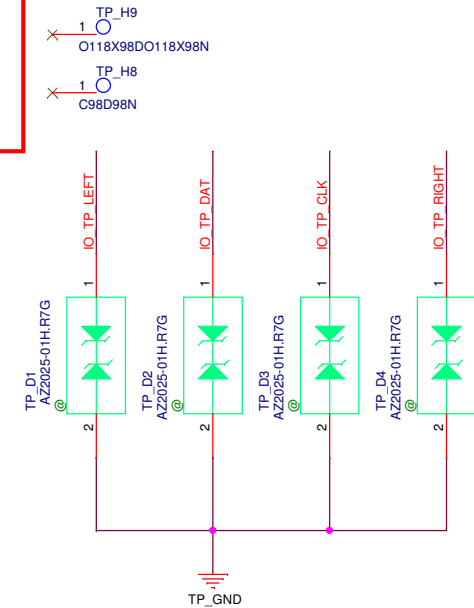
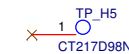
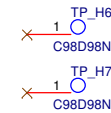
[illegible]

M : 1209-01B0000
S : 1209-019M000

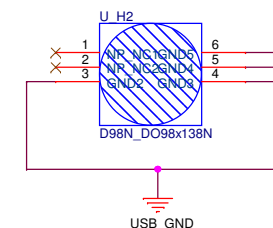
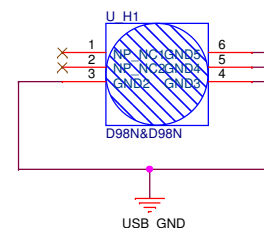
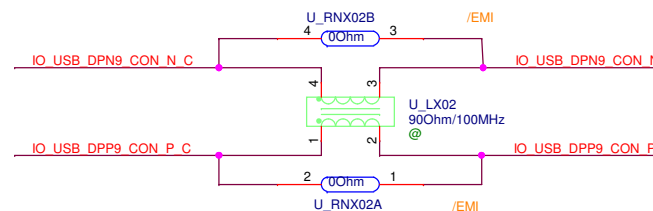
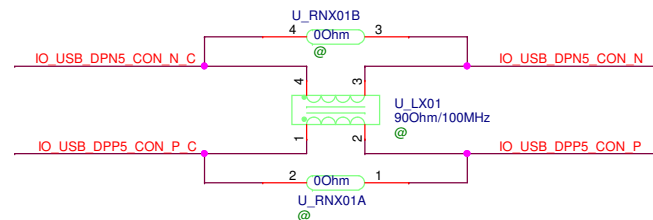
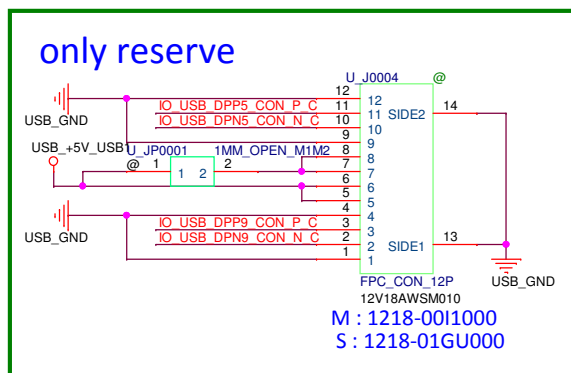
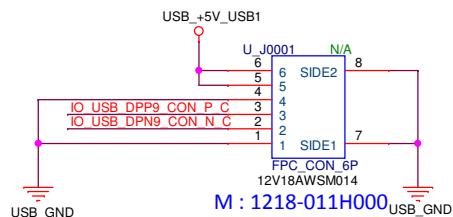
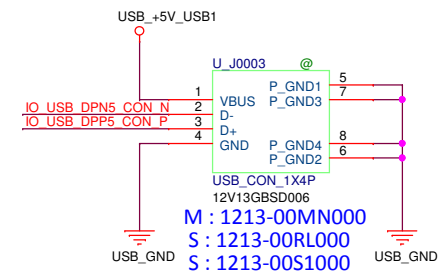
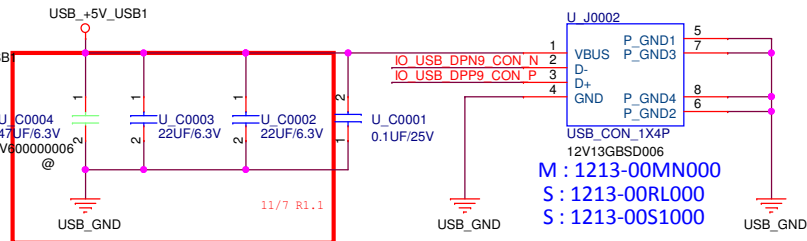
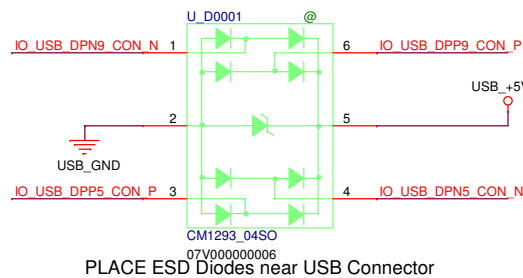


M : 1209-01B0000
S : 1209-019M000

R1.1



PEGATRON		Title : TP	
BG1-HW R&D Dept.3		Engineer: Tina Lee	
Size B	Project Name PT10SG	Rev 1.1	
Date: Tuesday, February 26, 2013		Sheet	101 of 102



PEGATRON		Title :IO_USB	
BG1-HW R&D Dept.3		Engineer: Tina Lee	
Size B	Project Name	PT10SG	Rev 1.1
Date: Tuesday, February 26, 2013	Sheet	102	of 102